TEXAS INSTRUMENTS

LMH3404

SBOS739A – MAY 2016 – REVISED JUNE 2016

LMH3404 Dual-Channel, 7-GHz, Low-Noise, Low-Power, Fully Differential Amplifier

1 Features

- 3-dB Bandwidth: 7 GHz
- Excellent Linearity Performance: DC to 2 GHz
- Fixed Differential-to-Differential Gain: 20 dB
- Channel Gain Matching DC to 1 GHz: < 0.05 dB
- Channel Phase Matching DC to 1 GHz: < 0.7°
- Crosstalk at 1 GHz: –70 dBc
- Slew Rate: 17,500 V/µs
- Low Harmonic Distortion ($2\text{-}V_{PP}$, 200-Ω, Diff-Diff Configuration):
  - 500 MHz: HD2 at –78 dBc, HD3 at –78 dBc
  - 1 GHz: HD2 at –65 dBc, HD3 at –72 dBc
  - 2 GHz: HD2 at –51 dBc, HD3 at –47 dBc
- Low Intermodulation Distortion ($2\text{-}V_{PP}$, 200-Ω, Diff-Diff Configuration):
  - 500 MHz: IMD2 at –85 dBc, IMD3 at –88 dBc
  - 1 GHz: IMD2 at –65 dBc, IMD3 at –71 dBc
  - 2 GHz: IMD2 at –51 dBc, IMD3 at –51 dBc
- Input Voltage Noise: 1.3 nV/$\sqrt{\text{Hz}}$
- Supports Single- and Dual-Supply Operation
- Power Consumption: 56 mA per Channel
- Power-Down Feature

2 Applications

- GSPS ADC Drivers
- IQ Demodulation Receivers
- ADC Drivers for Ultra Wide-Band or Narrow-Band Data Acquisition
- Single-Ended to Differential Signal Conversions
- DAC Buffers
- IF, RF, and Baseband Gain Blocks
- SAW Filter Buffers and Drivers
- Balun Replacement DC to 2 GHz
- Level Shifters

3 Description

The LMH3404 is a very high-performance, dual-channel, differential amplifier optimized for radio-frequency (RF), intermediate-frequency (IF), or high-speed time-domain applications. This device is ideal for dc- or ac-coupled applications that use differential-to-differential (Diff-Diff) or single-ended-to-differential (SE-Diff) conversion when driving an analog-to-digital converter (ADC). The LMH3404 generates very low levels of second- and third-order distortion when operating in SE-Diff or Diff-Diff mode.

The device has unprecedented usable bandwidth from dc to 2 GHz. The LMH3404 can be used as a very wide-band ADC driver, and also for SE-Diff conversions in the signal chain, without external baluns. The LMH3404 performance is ideal for a wide range of applications, such as test and measurement, broadband communications, and high-speed data acquisition.

A common-mode reference input pin is provided to align the amplifier output common-mode with the ADC input requirements. Power supplies between 3.15 V and 5.25 V can be selected, and dual-supply operation is supported when required by the application. A power-down feature is also available for saving power. This level of performance is achieved at a very low power level of 280 mW per channel when a 5.0-V supply is used.

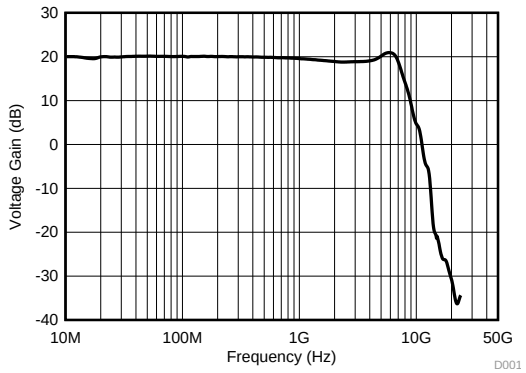
The LMH3404 is fabricated using Texas Instruments' advanced complementary BiCMOS process, and is available in a space-saving, 24-pin, VQFN package for higher performance.

Device Information(1)

DEVICE NAME	PACKAGE	BODY SIZE
LMH3404	VQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

LMH3404 Differential Small-Signal Frequency Response



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

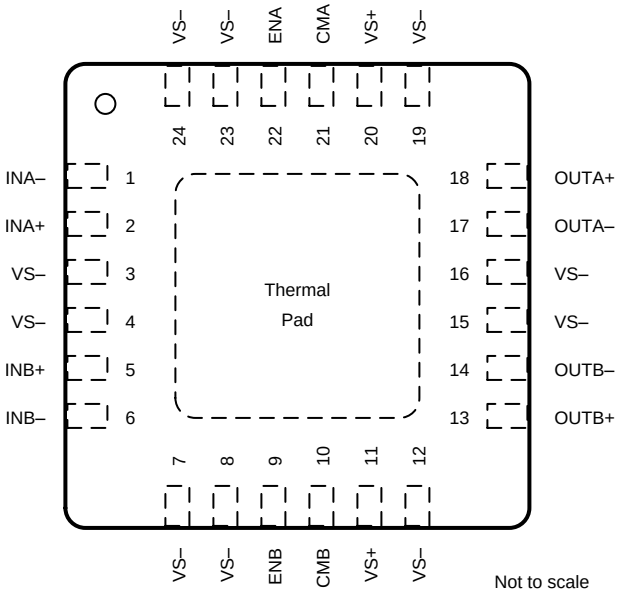
Changes from Original (May 2016) to Revision A	Page
• Changed from product preview to production data	1

5 Device Comparison Table

DEVICE	BW, GAIN	DISTORTION	NOISE (nV/√Hz)
LMH3401	7 GHz, A_V = 6.3 V/V	–79-dBc HD2, –77-dBc HD3 at 500 MHz	1.4
LMH5401	6 GHz, A_V = 12 V/V	–80-dBc HD2, –77-dBc HD3 at 500 MHz	1.25
LMH6554	1.6 GHz, A_V = 12 V/V	–79-dBc HD2, –70-dBc HD3 at 250 MHz	0.9

6 Pin Configuration and Functions

RGE Package
24-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CMA	21	I	This pin sets channel A output common-mode voltage. No internal bias; connect externally.
CMB	10	I	This pin sets channel B output common-mode voltage. No internal bias; connect externally.
ENA	22	I	Enable channel A (logic 1 = enabled). This pin is pulled-up internally.
ENB	9	I	Enable channel B (logic 1 = enabled). This pin is pulled-up internally.
INA–	1	I	Negative input pin for channel A
INA+	2	I	Positive input pin for channel A
INB–	6	I	Negative input pin for channel B
INB+	5	I	Positive input pin for channel B
OUTA–	17	O	Negative output pin for channel A
OUTA+	18	O	Positive output pin for channel A
OUTB–	14	O	Negative output pin for channel B
OUTB+	13	O	Positive output pin for channel B
VS–	3, 4, 7, 8, 12, 15, 16, 19, 23, 24	P	Negative supply voltage
VS+	11, 20	P	Positive supply voltage
Thermal pad			Thermal pad, ground reference for ENA and ENB pins. Connect exposed thermal pad to printed circuit board (PCB) ground plane.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Power supply		5.5	V
	Input voltage	$(V_{S–})$ – 0.7	(V_{S+}) + 0.7	V
Current	Input current		10	mA
	Output current (sourcing or sinking) OUT+, OUT–		100	mA
Temperature	Operating free-air, T_A	–40	85	°C
	Junction, T_J		150	°C
	Storage, T_{stg}	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage ($V_S = V_{S+} – V_{S–}$)	3.15	5	5.25	V
Junction temperature, T_J	–40		125	°C
Operating free-air temperature, T_A	–40	25	85	°C

7.4 Thermal Information

THERMAL METRIC(1)		LMH3404 RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: V_S = 5 V

at T_A = 25°C, V_S = ±2.5 V, V_{CMx} = V_{CMA} or V_{CMB} = 0 V, R_L = 200-Ω differential, differential input and output, output measured at OUT_AMP reference point (see *Output Reference Points* section), and input and output referred to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_{OD} = 200 mV_{PP}		7		GHz	C
LSBW	Large-signal bandwidth	V_{OD} = 2 V_{PP}		6.5		GHz	C
	Bandwidth for 0.1-dB flatness	V_{OD} = 2 V_{PP}		700		MHz	C
SR	Slew rate	V_{OD} = 2-V step		17500		V/µs	C
	Rise time	V_{OD} = 1-V step		80		ps	C
	Fall time	V_{OD} = 1-V step		80		ps	C
	Settling time to 1%	V_{OD} = 2-V step		1		ns	C
S11	Input return loss	100-Ω matched input, f < 1 GHz		–20		dB	C
HD2	Second-order harmonic distortion	f = 10 MHz, V_{OD} = 2 V_{PP}		–90		dBc	C
		f = 500 MHz, V_{OD} = 2 V_{PP}		–84		dBc	C
		f = 1 GHz, V_{OD} = 2 V_{PP}		–64		dBc	C
		f = 2 GHz, V_{OD} = 2 V_{PP}		–51		dBc	C
HD3	Third-order harmonic distortion	f = 10 MHz, V_{OD} = 2 V_{PP}		–100		dBc	C
		f = 500 MHz, V_{OD} = 2 V_{PP}		–93		dBc	C
		f = 1 GHz, V_{OD} = 2 V_{PP}		–69		dBc	C
		f = 2 GHz, V_{OD} = 2 V_{PP}		–47		dBc	C
IMD2	Second-order intermodulation distortion	f = 10 MHz, V_{OD} = 1 V_{PP} per tone		–89		dBc	C
		f = 500 MHz, V_{OD} = 1 V_{PP} per tone		–77		dBc	C
		f = 1 GHz, V_{OD} = 1 V_{PP} per tone		–67		dBc	C
		f = 2 GHz, V_{OD} = 1 V_{PP} per tone		–51		dBc	C
IMD3	Third-order intermodulation disortion	f = 10 MHz, V_{OD} = 1 V_{PP} per tone		–95		dBc	C
		f = 500 MHz, V_{OD} = 1 V_{PP} per tone		–95		dBc	C
		f = 1 GHz, V_{OD} = 1 V_{PP} per tone		–72		dBc	C
		f = 2 GHz, V_{OD} = 1 V_{PP} per tone		–51		dBc	C
OIP3	Output third-order intercept point	f = 200 MHz, at device outputs		50		dBm	C
		f = 1 GHz, at device outputs		35		dBm	C
e_n	Voltage noise	f = 100 MHz, referred to input pins(2)		1.3		nV/√Hz	C
	Internal voltage noise			1.25		nV/√Hz	C
NF	Noise figure	f = 500 MHz, at device outputs, 100-Ω source		6.6		dB	C
		f = 1 GHz, at device outputs, 100-Ω source		6.9		dB	C
	Output balance error	f = 1 GHz		–45		dBc	C
z_o	Output impedance	f = dc, differential	16	20	24	Ω	A
DC PERFORMANCE							
	Gain	100-Ω differential source, referred to input pins	19.8	20	20.2	dB	A
	Differential output offset	T_A = 25°C		±2	±40	mV	A
		T_A = –40°C to +85°C		±5		mV	C
	Differential output offset temperature drift			20		µV/°C	C
CMRR	Common-mode rejection ratio	f = 100 MHz, T_A = 25°C		66		dB	C

(1) Test levels: (A) 100% tested at 25°C. Overtemperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Voltage noise measured at device input pins (see *Noise Analysis* section).

Electrical Characteristics: V_S = 5 V (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CMx} = V_{CMA} or V_{CMB} = 0 V, R_L = 200-Ω differential, differential input and output, output measured at OUT_AMP reference point (see *Output Reference Points* section), and input and output referred to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
INPUT							
	Differential input resistance		80	100	120	Ω	A
	Differential input capacitance			0.3		pF	C
	Input common-mode low	Inputs shorted together, V_{CMx} = 2.5 V, referenced to device pin		$V_{S–}$	$V_{S–}$ + 0.2	V	A
	Input common mode high	Inputs shorted together, V_{CMx} = 2.5 V, referenced to device pin	V_{S+} – 1.3	V_{S+} – 1.2		V	A
OUTPUT							
	Output voltage high	T_A = 25°C, measured single ended	V_{S+} – 1.2	V_{S+} – 0.95		V	A
		T_A = –40°C to +85°C, measured single ended		V_{S+} – 1.1		V	C
	Output voltage low	T_A = 25°C, measured single ended	$V_{S–}$ + 1.2	$V_{S–}$ + 0.95		V	A
		T_A = –40°C to +85°C, measured single ended		$V_{S–}$ + 1.2		V	C
V_{OD}	Differential output voltage, (V_{OUTx+}) – ($V_{OUTx–}$)			5.6		V_{PP}	C
	Differential output current drive	V_{OD} = 0 V	40	50		mA	A
OUTPUT COMMON MODE CONTROL (CMA AND CMB PINS)							
	V_{CMx} small-signal bandwidth	V_{OCM} = 200 mV_{PP}		3.3		GHz	C
	V_{CMx} slew rate	V_{OCM} = 500 mV_{PP}		2900		V/µs	C
	V_{CMx} voltage low	Differential gain shift < 1 dB		$V_{S–}$ +1.6	$V_{S–}$ + 2.0	V	A
	V_{CMx} voltage high	Differential gain shift < 1 dB	V_{S+} – 2.0	V_{S+} – 1.6		V	A
	V_{CMx} gain		0.98	1	1.01	V/V	A
	V_{OCM} output common-mode offset from V_{CMx} input voltage (3)		–50	0	50	mV	A
	V_{CMx} temperature drift	f = dc		40		µV/°C	C
	V_{CMx} input current high			12		µA	C
POWER SUPPLY							
I_Q	Quiescent current per channel	T_A = 25°C	51	56	64	mA	A
PSRR	Power-supply rejection ratio	f = dc, VS+	60	84		dB	A
		f = dc, VS–	50	75		dB	A
POWER DOWN (ENA AND ENB PINS)							
V_T	Enable or disable voltage threshold	Device powers down below 0.9 V, device powers on above 1.2 V	0.9	1.1	1.2	V	A
	Power-down quiescent current per channel	V_{EN} = 0 V	1	3	6	mA	A
	Enable (EN) pin bias current	V_{EN} = 0 V		-50		µA	C
	Turn-on time delay	Time to V_{OD} = 90% of final value		10		ns	C
	Turn-off time delay	Time to V_{OD} = 10% of original value		10		ns	C
CHANNEL MATCHING							
	Gain matching	f = dc		0.04	0.06	dB	A
		f < 1 GHz		0.05		dB	C
	Phase matching	f < 1 GHz		0.7		°	C
	Gain matching drift	T_A = 25°C ±10°C, f = dc		0.01		dB	C
	Crosstalk	f = 1 GHz		–70		dBc	C

(3) V_{OCM} = (V_{OUTx+} + $V_{OUTx–}$) / 2.

7.6 Electrical Characteristics: V_S = 3.3 V

at T_A = 25°C, V_S = ±1.65 V, V_{CMx} = V_{CMA} or V_{CMB} = 0 V, R_L = 200-Ω differential, differential input and output, output measured at OUT_AMP reference point (see *Output Reference Points* section), and input and output referred to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_{OD} = 200 mV_{PP}		7		GHz	C
LSBW	Large-signal bandwidth	V_{OD} = 2 V_{PP}		6		GHz	C
	Bandwidth for 0.1-dB flatness	V_{OD} = 2 V_{PP}		500		MHz	C
SR	Slew rate	V_{OD} = 2-V step		17600		V/µs	C
	Rise time	V_{OD} = 1-V step		90		ps	C
	Fall time	V_{OD} = 1-V step		90		ps	C
	Settling time to 1%	V_{OD} = 2-V step		1		ns	C
S11	Input return loss	100-Ω matched input, f < 1 GHz		-20		dB	C
HD2	Second-order harmonic distortion	f = 500 MHz, V_{OD} = 1 V_{PP}		-62		dBc	C
HD3	Third-order harmonic distortion	f = 500 MHz, V_{OD} = 1 V_{PP}		-85		dBc	C
	Output balance error	f = 1 GHz		-46		dBc	C
z_o	Output impedance	f = dc	16	20	24	Ω	A
DC PERFORMANCE							
	Gain	100-Ω differential source, referred to input pins	19.8	20	20.2	dB	A
	Differential output offset	T_A = 25°C		±2	±40	mV	A
		T_A = –40°C to +85°C		±5		mV	C
	Differential output offset temperature drift			20		µV/°C	C
CMRR	Common-mode rejection ratio	f = 100 MHz, T_A = 25°C		60		dBc	C
INPUT							
	Input common-mode low	Inputs shorted together, V_{CMx} = 2.5 V, referenced to device pin		$V_{S–}$	$V_{S–}$ + 0.2	V	A
	Input common mode high	Inputs shorted together, V_{CMx} = 2.5 V, referenced to device pin	V_{S+} – 1.5	V_{S+} – 1.6		V	A
OUTPUT							
	Output voltage high	T_A = 25°C, measured single ended	V_{S+} – 1.2	V_{S+} – 0.95		V	A
		T_A = –40°C to +85°C, measured single ended		V_{S+} – 1.05		V	C
	Output voltage low	T_A = 25°C, measured single ended	$V_{S–}$ + 1.2	$V_{S–}$ + 0.95		V	A
		T_A = –40°C to +85°C, measured single ended		$V_{S–}$ + 1.05		V	C
V_{OD}	Differential output voltage (V_{OUTx+}) – ($V_{OUTx–}$)			2.4		V_{PP}	C
	Differential output current drive	V_O = 0 V	30	40		mA	A

(1) Test levels: (A) 100% tested at 25°C. Overtemperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

Electrical Characteristics: V_S = 3.3 V (continued)

at T_A = 25°C, V_S = ±1.65 V, V_{CMx} = V_{CMA} or V_{CMB} = 0 V, R_L = 200-Ω differential, differential input and output, output measured at OUT_AMP reference point (see *Output Reference Points* section), and input and output referred to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
OUTPUT COMMON-MODE CONTROL (CMA AND CMB PINS)							
	V_{CMx} small-signal bandwidth	V_{OCM} = 200 mV_{PP}		3.3		GHz	C
	V_{CMx} slew rate	V_{OCM} = 500 mV_{PP}		2600		V/µs	C
	V_{CMx} voltage range low	Differential gain shift < 1 dB		$V_{S–}$ +1.35	$V_{S–}$ + 1.55	V	A
	V_{CMx} voltage range high	Differential gain shift < 1 dB	V_{S+} – 1.55	V_{S+} – 1.35		V	A
	V_{CMx} gain	V_{CMx} = 0 V	0.98	1	1.01	V/V	A
	V_{OCM} output common-mode offset from V_{CMx} input voltage (2)	V_{CMx} = 0 V		20		mV	C
	V_{CMx} temperature drift	f = dc		40		µV/°C	C
POWER SUPPLY							
I_Q	Quiescent current per channel	T_A = 25°C	47	54	61	mA	A
PSRR	Power-supply rejection ratio	f = dc, VS+	60	84		dB	A
		f = dc, VS–	50	75		dB	A
POWER DOWN (ENA AND ENB PINS)							
V_T	Enable or disable voltage threshold	Device powers down below 1 V, device powers on above 1.2 V	1	1.1	1.2	V	A
	Power-down quiescent current per channel	V_{EN} = 0 V	1	1.6	5	mA	A
	Turn-on time delay	Time to V_{OD} = 90% of final value		10		ns	C
	Turn-off time delay	Time to V_{OD} = 10% of original value		10		ns	C
CHANNEL MATCHING							
	Gain matching	f = dc		0.04	0.06	dB	A
		f < 1 GHz		0.05		dB	C
	Phase matching	f < 1 GHz		0.7		°	C
	Gain matching drift	T_A = 25°C ±10°C, f = dc		0.01		dB	C

(2) $V_{OCM} = (V_{OUTx+} + V_{OUTx–}) / 2$

7.7 Typical Characteristics: V_S = 5 V

At T_A = 25°C, V_S = ±2.5 V, V_{CMx} = V_{CMA} or V_{CMB} = 0 V, R_L = 200-Ω differential, differential input and differential output, output measured at OUT_AMP reference point (see *Output Reference Points* section), and input and output pins referenced to midsupply (unless otherwise noted). Plot data measured using an EVM, as discussed in the *Parameter Measurement Information* section (see Figure 61 to Figure 63).

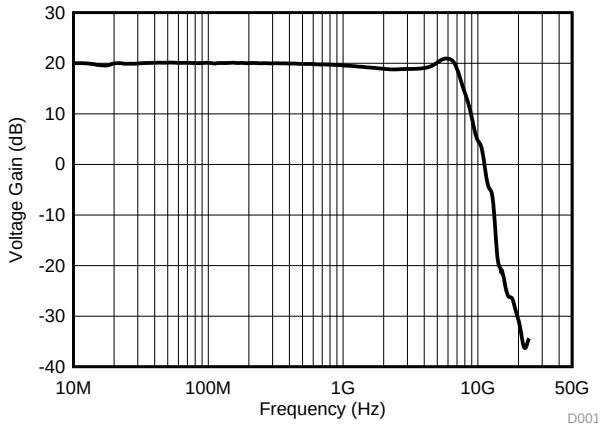


Figure 1. Small-Signal Frequency Response

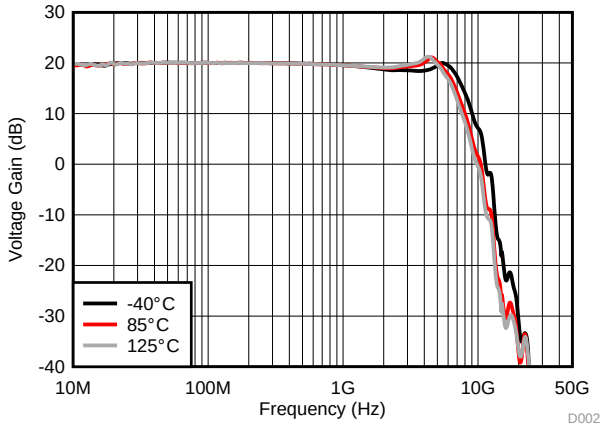


Figure 2. Small-Signal Frequency Response vs Temperature

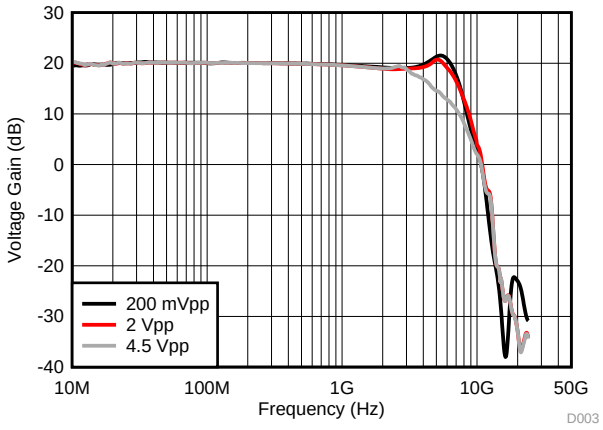


Figure 3. Frequency Response vs Output Power

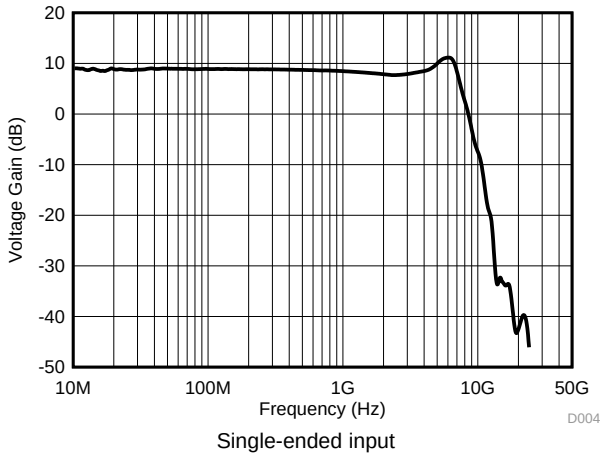


Figure 4. Small-Signal Frequency Response

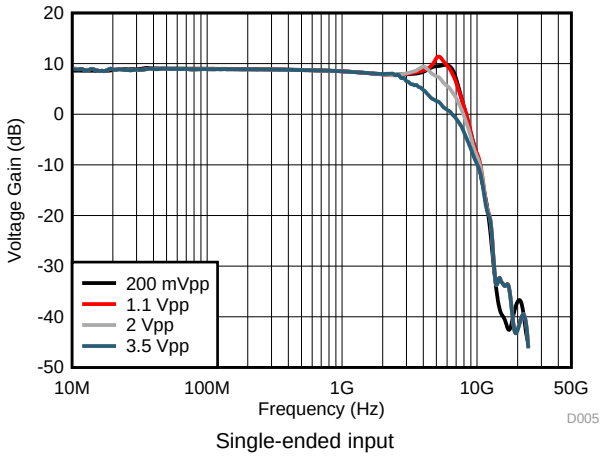


Figure 5. Frequency Response vs Output Power

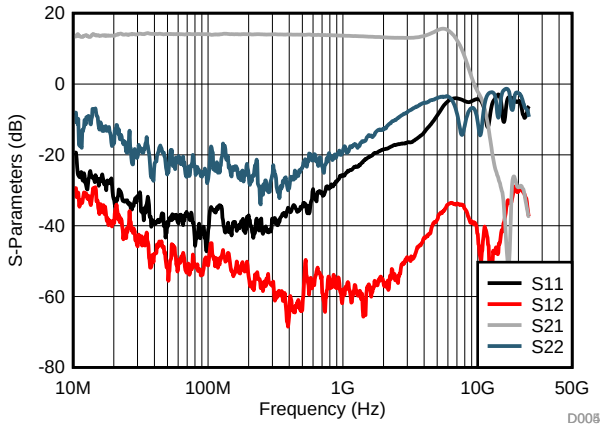
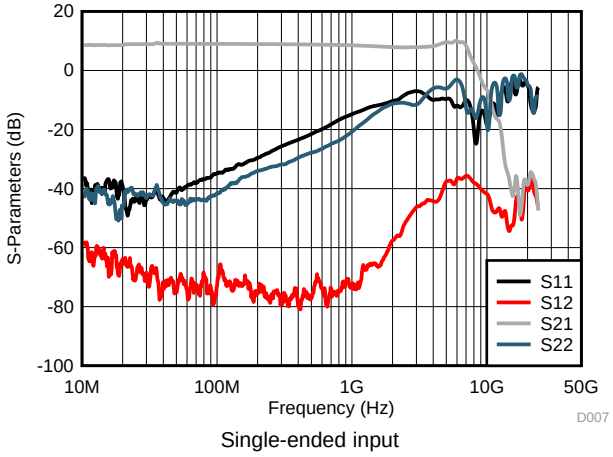


Figure 6. S-Parameters

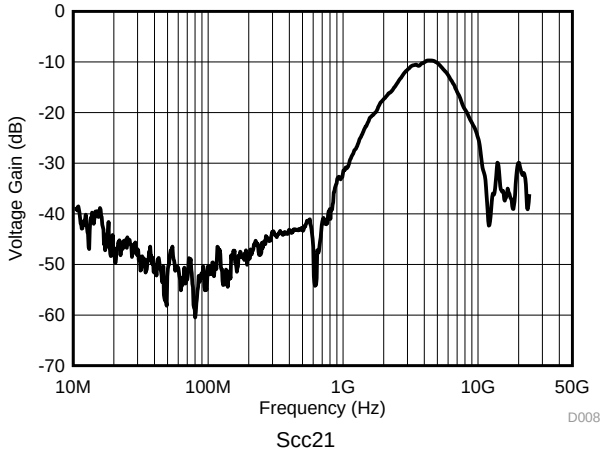
Typical Characteristics: V_S = 5 V (continued)

At T_A = 25°C, V_S = ±2.5 V, V_{CMx} = V_{CMA} or V_{CMB} = 0 V, R_L = 200-Ω differential, differential input and differential output, output measured at OUT_AMP reference point (see *Output Reference Points* section), and input and output pins referenced to midsupply (unless otherwise noted). Plot data measured using an EVM, as discussed in the *Parameter Measurement Information* section (see Figure 61 to Figure 63).



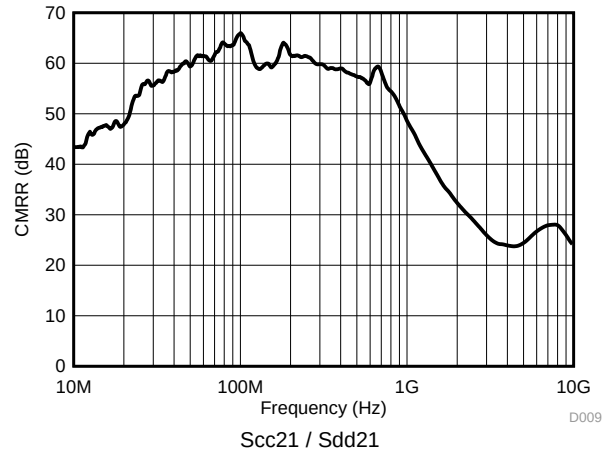
Single-ended input

Figure 7. S-Parameters



Scc21

Figure 8. Common-Mode Frequency Response



Scc21 / Sdd21

Figure 9. Common-Mode Rejection Ratio

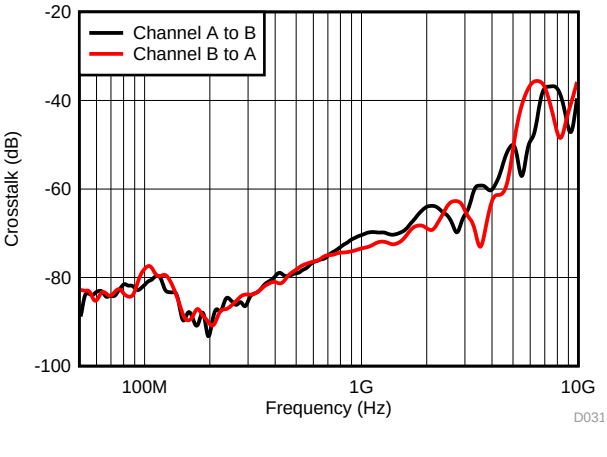
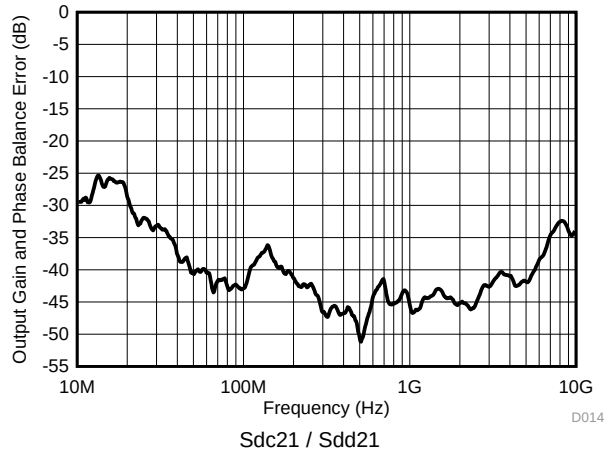
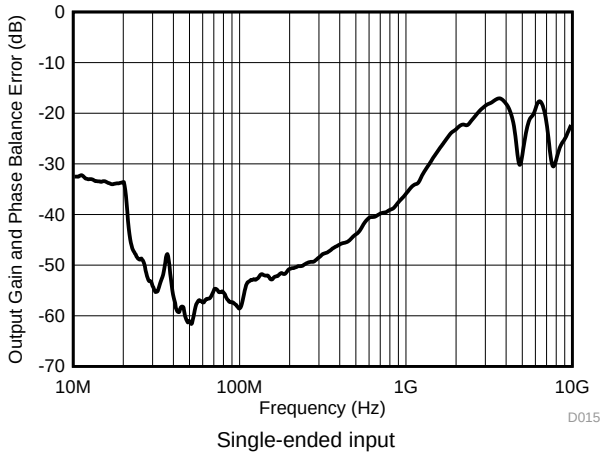


Figure 10. Crosstalk



Sdc21 / Sdd21

Figure 11. Output-Balance Error



Single-ended input

Figure 12. Output-Balance Error

Typical Characteristics: V_S = 5 V (continued)

At T_A = 25°C, V_S = ±2.5 V, V_{CMx} = V_{CMA} or V_{CMB} = 0 V, R_L = 200-Ω differential, differential input and differential output, output measured at OUT_AMP reference point (see *Output Reference Points* section), and input and output pins referenced to midsupply (unless otherwise noted). Plot data measured using an EVM, as discussed in the *Parameter Measurement Information* section (see Figure 61 to Figure 63).

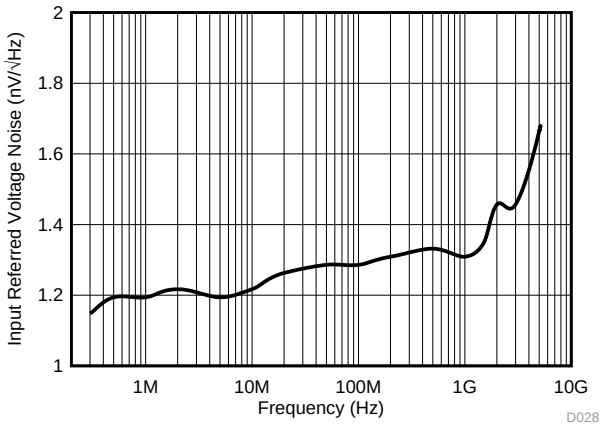


Figure 13. Input-Voltage Noise

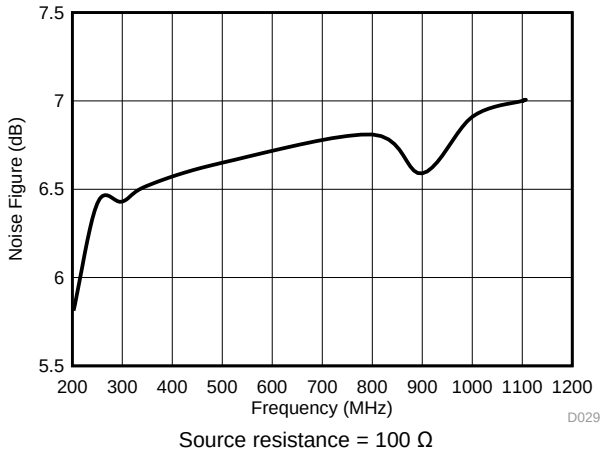


Figure 14. Noise Figure

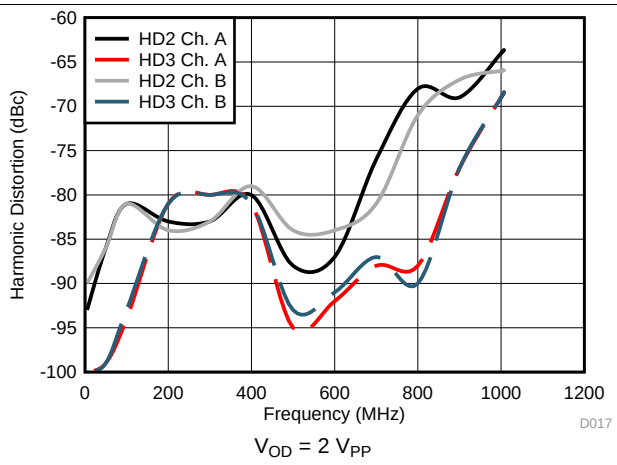


Figure 15. Harmonic Distortion

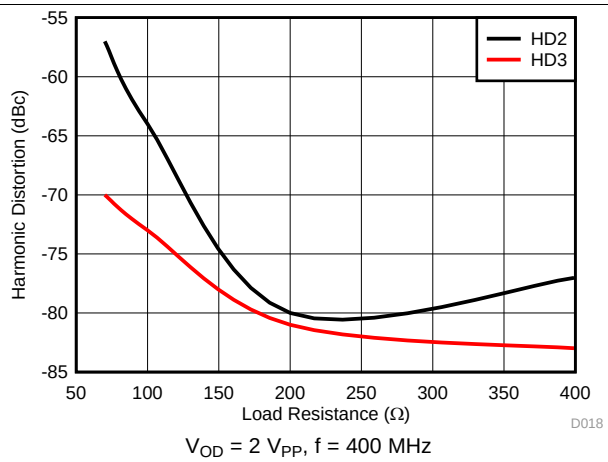


Figure 16. Harmonic Distortion vs Load Resistance

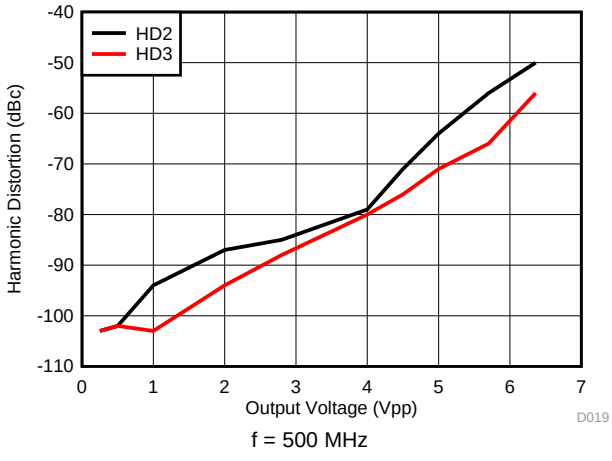


Figure 17. Harmonic Distortion vs Output Voltage

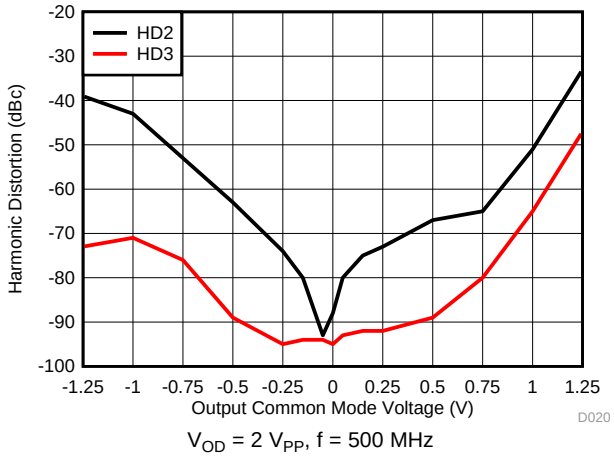
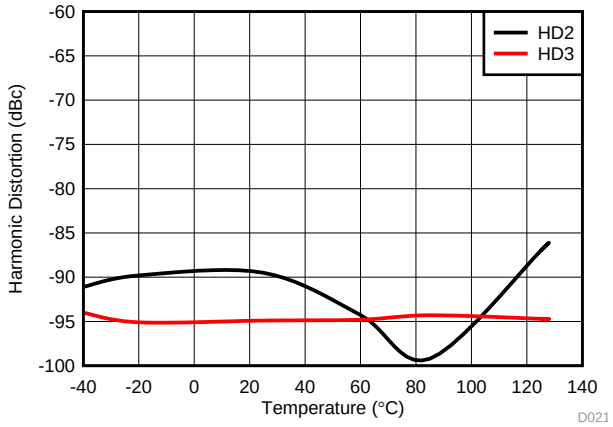


Figure 18. Harmonic Distortion vs Output Common-Mode Voltage

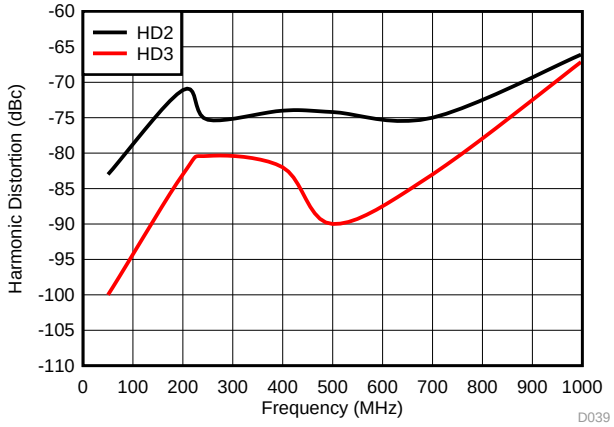
Typical Characteristics: V_S = 5 V (continued)

At T_A = 25°C, V_S = ±2.5 V, V_{CMx} = V_{CMA} or V_{CMB} = 0 V, R_L = 200-Ω differential, differential input and differential output, output measured at OUT_AMP reference point (see *Output Reference Points* section), and input and output pins referenced to midsupply (unless otherwise noted). Plot data measured using an EVM, as discussed in the *Parameter Measurement Information* section (see Figure 61 to Figure 63).



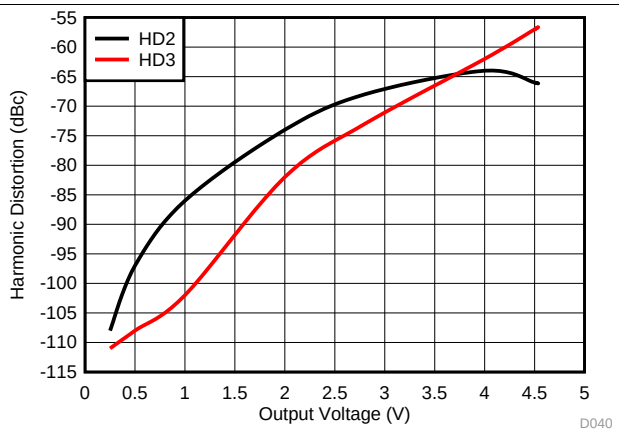
V_{OD} = 2 V_{PP}, f = 500 MHz

Figure 19. Harmonic Distortion vs Temperature



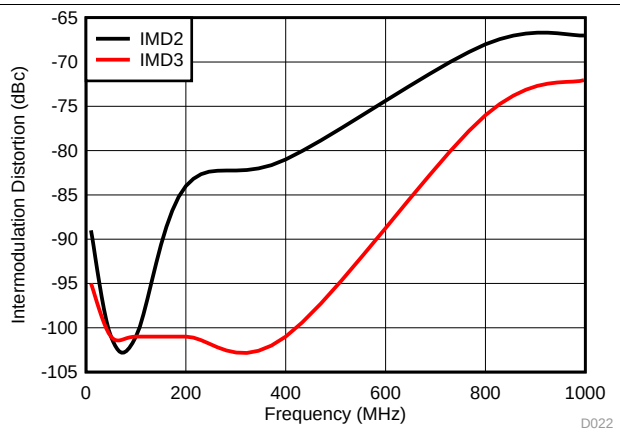
Single-ended input, V_{OD} = 2 V_{PP}

Figure 20. Harmonic Distortion



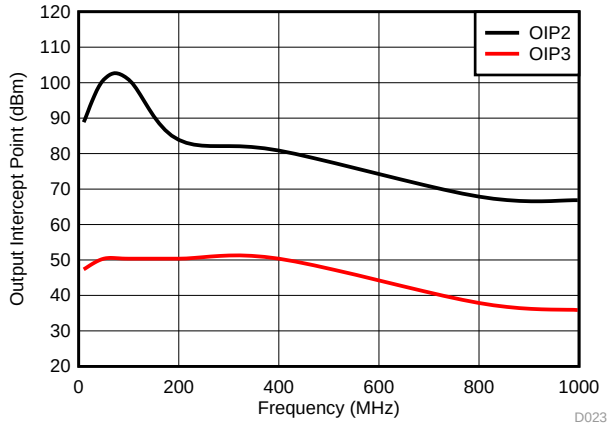
Single-ended input, f = 400 MHz

Figure 21. Harmonic Distortion vs Output Voltage



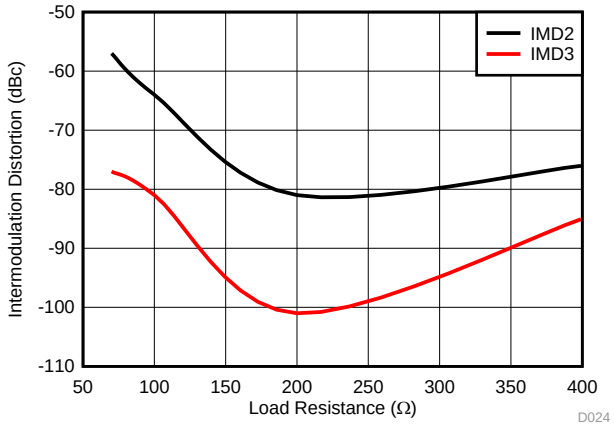
V_{OD} = 2-V_{PP} composite

Figure 22. Intermodulation Distortion



V_{OD} = 2-V_{PP} composite

Figure 23. Output Intercept Point

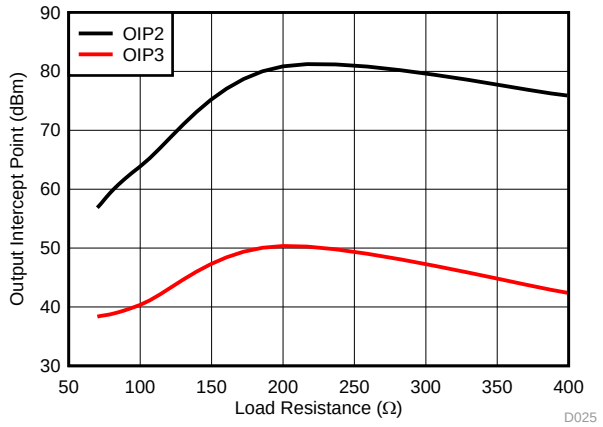


V_{OD} = 2-V_{PP} composite, center frequency = 400 MHz

Figure 24. Intermodulation Distortion vs Load

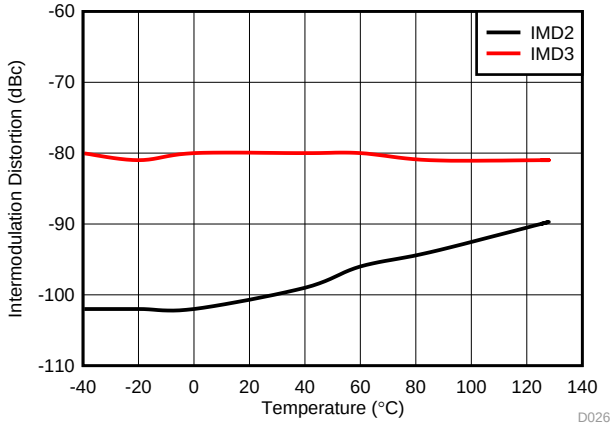
Typical Characteristics: V_S = 5 V (continued)

At T_A = 25°C, V_S = ±2.5 V, V_{CMx} = V_{CMA} or V_{CMB} = 0 V, R_L = 200-Ω differential, differential input and differential output, output measured at OUT_AMP reference point (see *Output Reference Points* section), and input and output pins referenced to midsupply (unless otherwise noted). Plot data measured using an EVM, as discussed in the *Parameter Measurement Information* section (see Figure 61 to Figure 63).



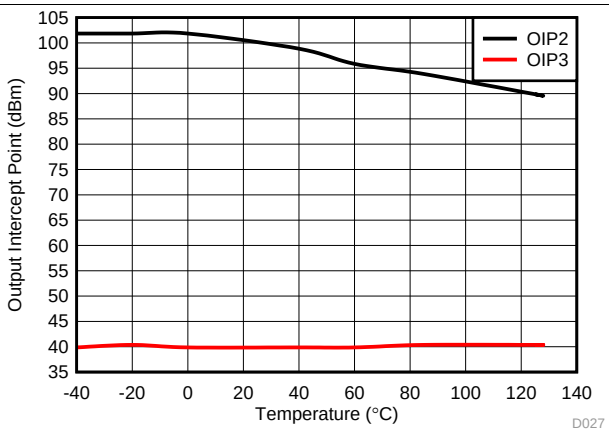
V_{OD} = 2-V_{PP} composite, center frequency = 400 MHz

Figure 25. Output Intercept Point vs Load



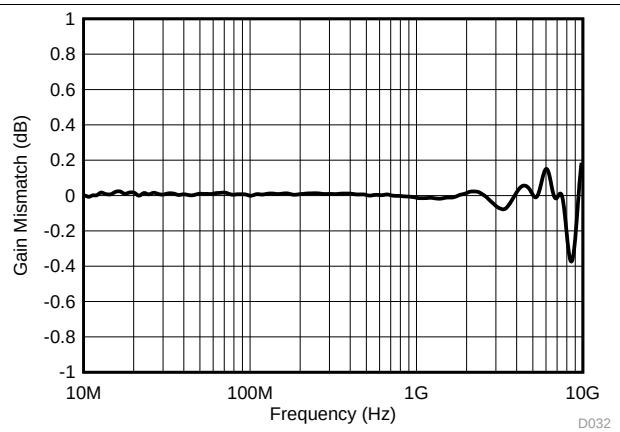
V_{OD} = 2-V_{PP} composite. center frequency = 400 MHz

Figure 26. Intermodulation Distortion vs Temperature



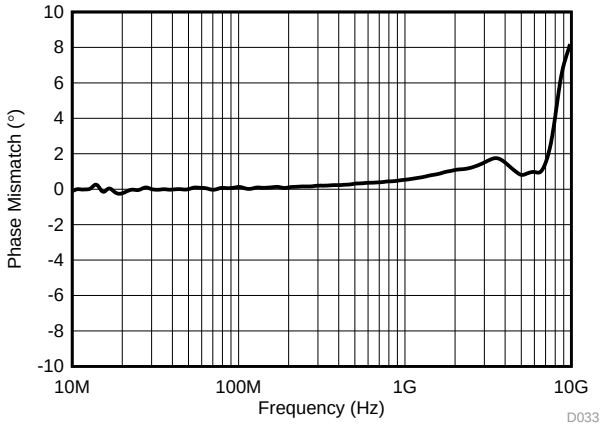
V_{OD} = 2-V_{PP} composite, center frequency = 400 MHz

Figure 27. Output Intercept vs Temperature



Channel-to-channel measurement

Figure 28. Gain Mismatch



Channel-to-channel measurement

Figure 29. Phase Mismatch

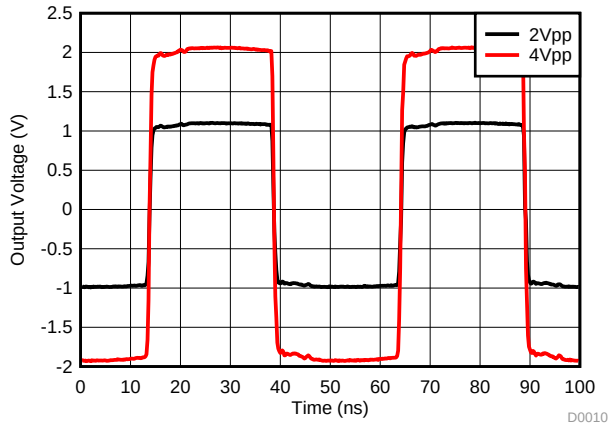


Figure 30. Pulse Response vs Output Voltage

Typical Characteristics: V_S = 5 V (continued)

At T_A = 25°C, V_S = ±2.5 V, V_{CMx} = V_{CMA} or V_{CMB} = 0 V, R_L = 200-Ω differential, differential input and differential output, output measured at OUT_AMP reference point (see *Output Reference Points* section), and input and output pins referenced to midsupply (unless otherwise noted). Plot data measured using an EVM, as discussed in the *Parameter Measurement Information* section (see Figure 61 to Figure 63).

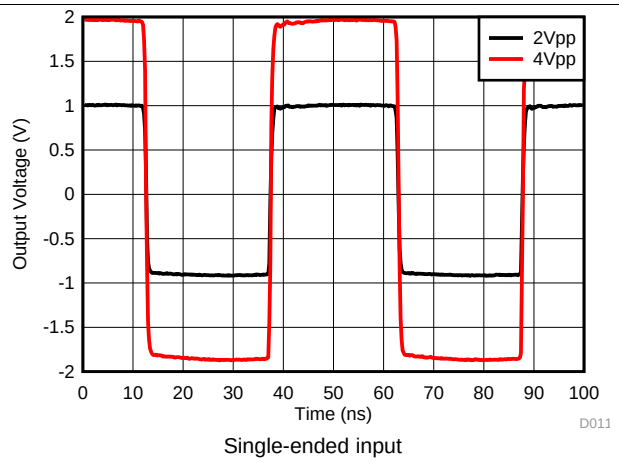


Figure 31. Pulse Response vs Output Voltage

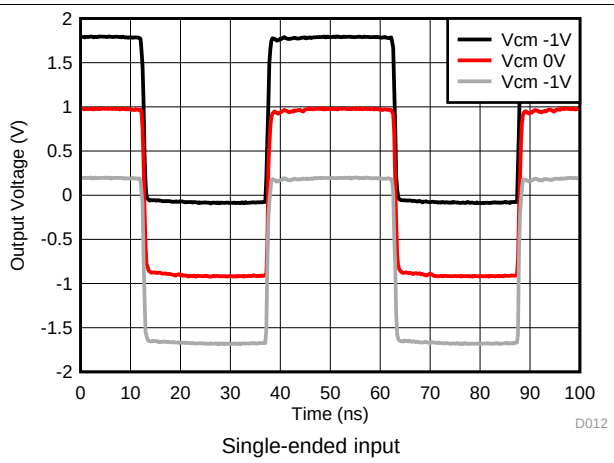


Figure 32. Pulse Response vs Output Common-Mode Voltage

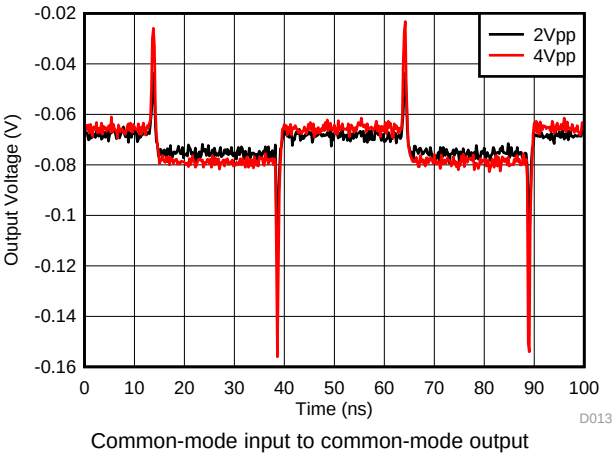


Figure 33. Common-Mode Pulse Response

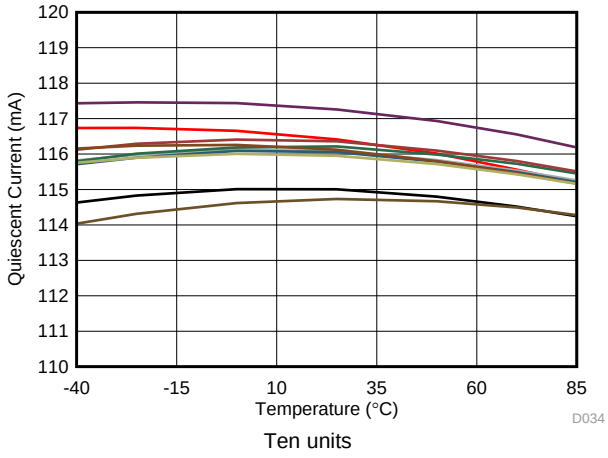


Figure 34. Quiescent Current vs Temperature

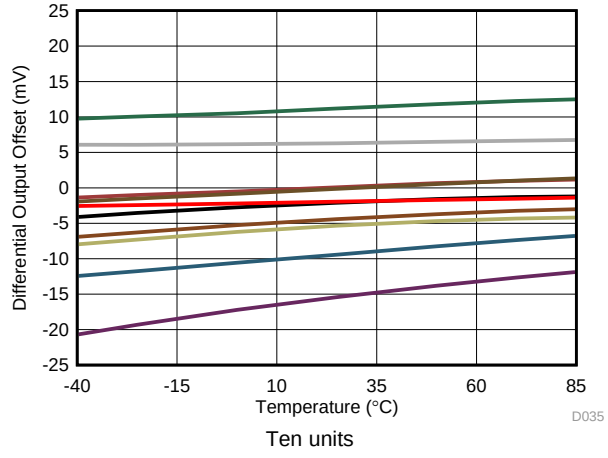


Figure 35. Output Offset Voltage vs Temperature

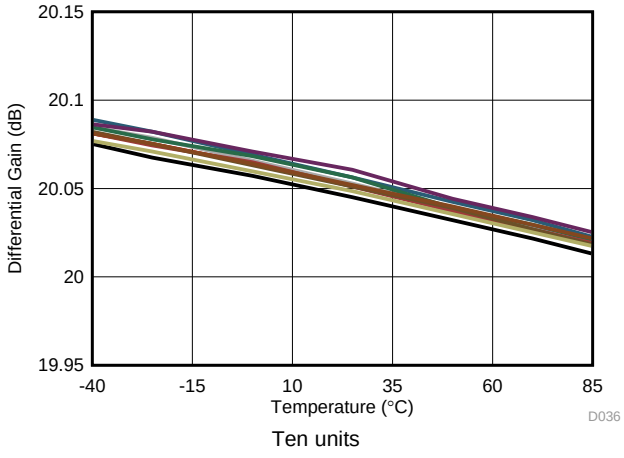


Figure 36. Gain vs Temperature

Typical Characteristics: V_S = 5 V (continued)

At T_A = 25°C, V_S = ±2.5 V, V_{CMx} = V_{CMA} or V_{CMB} = 0 V, R_L = 200-Ω differential, differential input and differential output, output measured at OUT_AMP reference point (see *Output Reference Points* section), and input and output pins referenced to midsupply (unless otherwise noted). Plot data measured using an EVM, as discussed in the *Parameter Measurement Information* section (see Figure 61 to Figure 63).

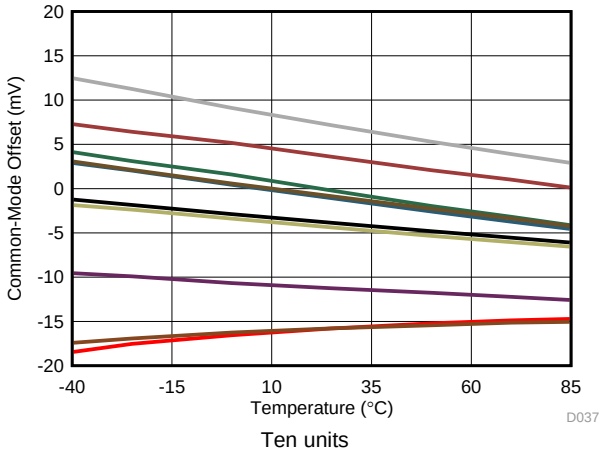


Figure 37. Common Mode Offset Voltage vs Temperature

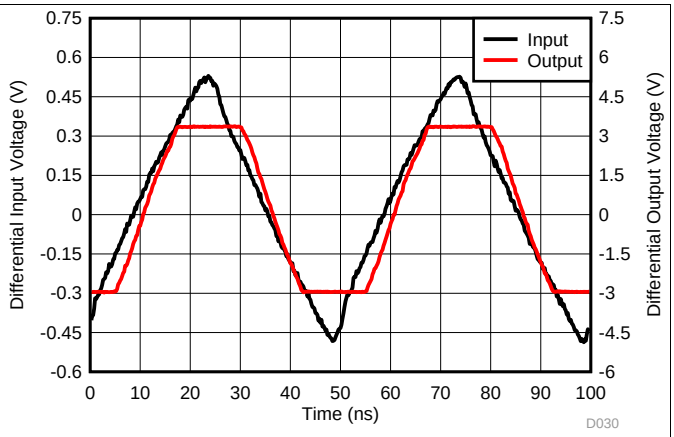


Figure 38. Overdrive Recovery

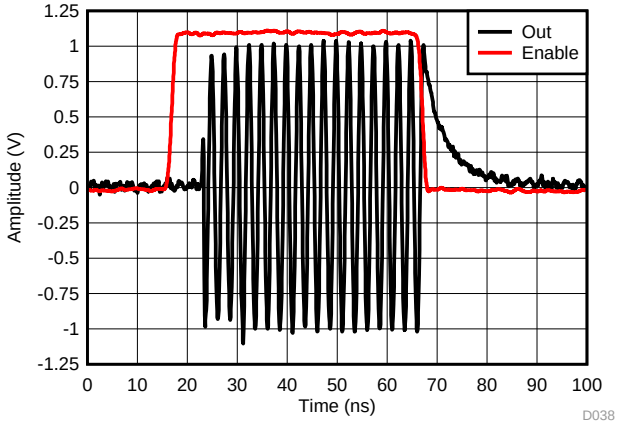


Figure 39. Enable Timing

7.8 Typical Characteristics: V_S = 3.3 V

At T_A = 25°C, V_S = ±1.65 V, V_{CMx} = V_{CMA} or V_{CMB} = 0 V, R_L = 200-Ω differential, differential input and differential output, output measured at OUT_AMP reference point (see *Output Reference Points* section), and input and output pins referenced to midsupply (unless otherwise noted). Plot data measured using an EVM, as discussed in the *Parameter Measurement Information* section (see Figure 61 to Figure 63).

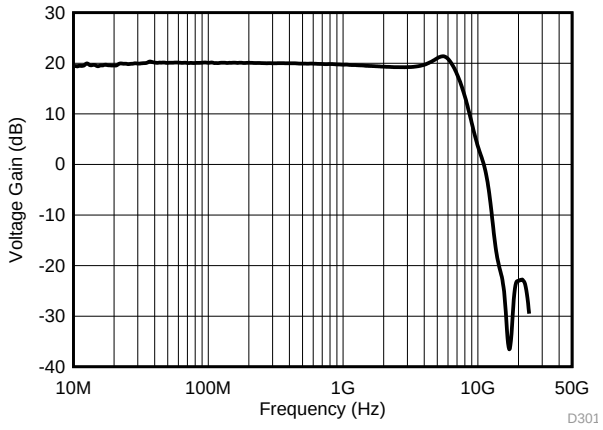
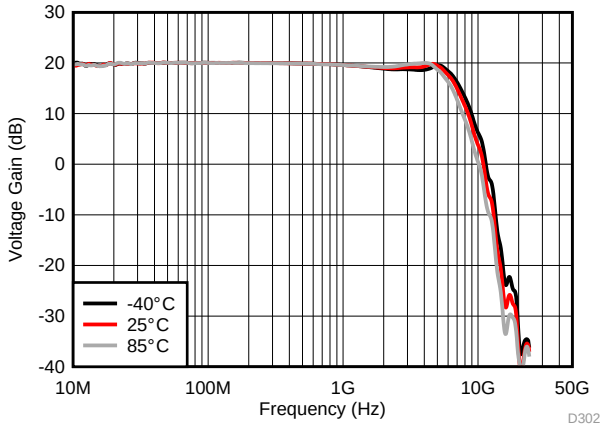


Figure 40. Small-Signal Frequency Response



V_{OD} = 2 V_{PP}

Figure 41. Frequency Response vs Temperature

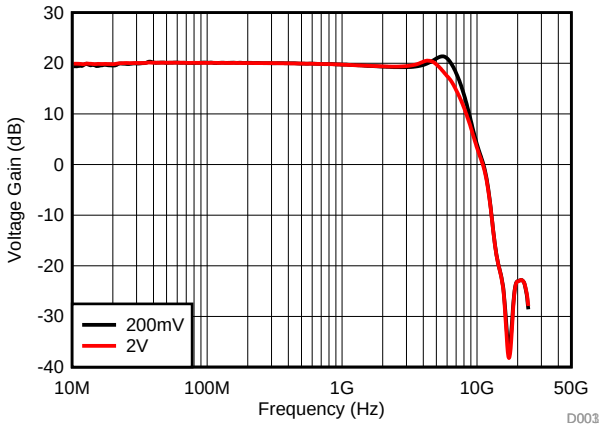
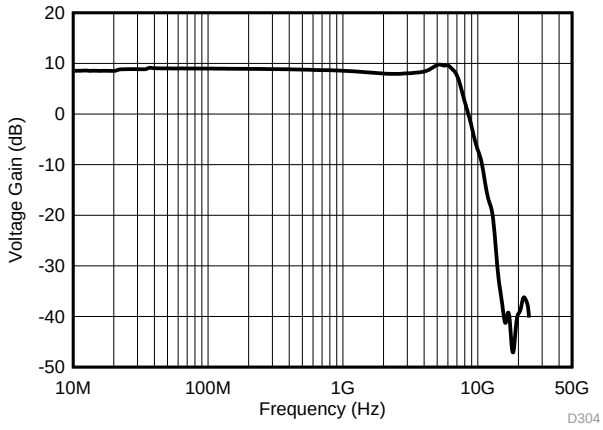
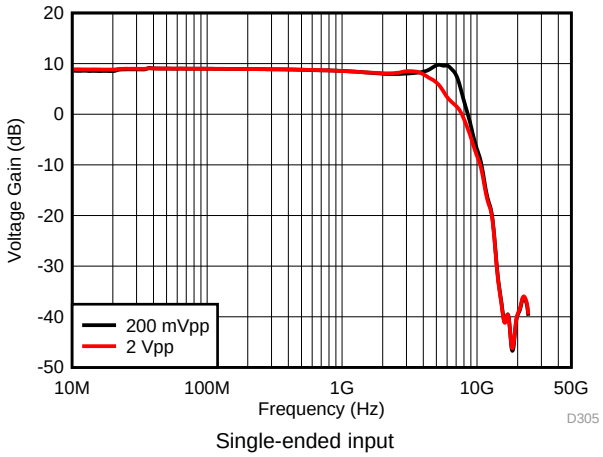


Figure 42. Frequency Response vs Output Power



Single-ended input

Figure 43. Small-Signal Frequency Response



Single-ended input

Figure 44. Frequency Response vs Output Swing

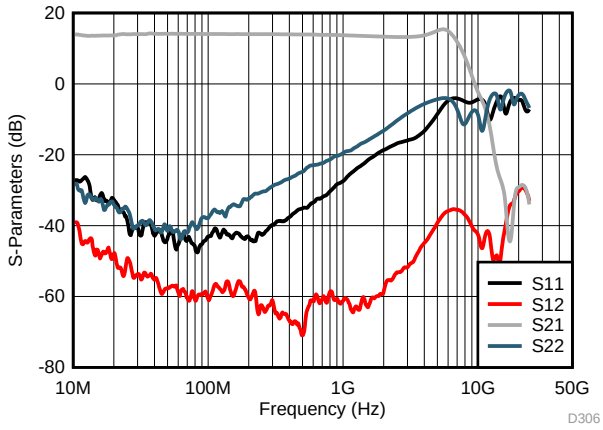
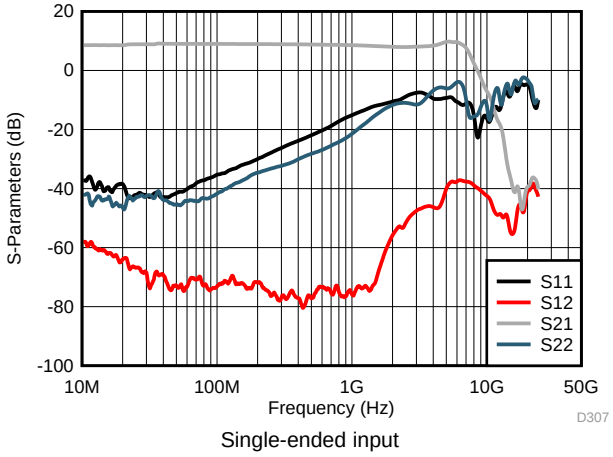


Figure 45. S-Parameters

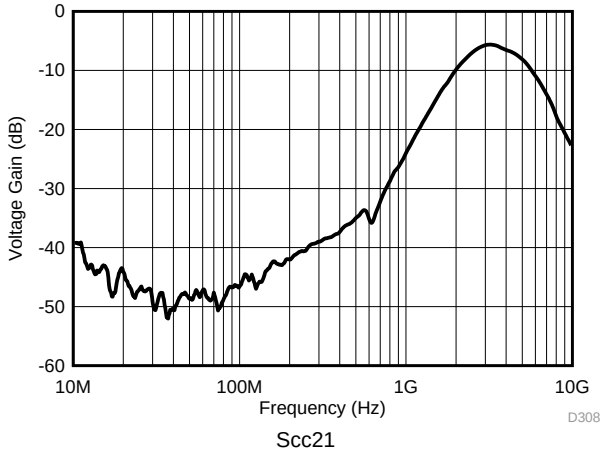
Typical Characteristics: V_S = 3.3 V (continued)

At T_A = 25°C, V_S = ±1.65 V, V_{CMx} = V_{CMA} or V_{CMB} = 0 V, R_L = 200-Ω differential, differential input and differential output, output measured at OUT_AMP reference point (see *Output Reference Points* section), and input and output pins referenced to midsupply (unless otherwise noted). Plot data measured using an EVM, as discussed in the *Parameter Measurement Information* section (see Figure 61 to Figure 63).



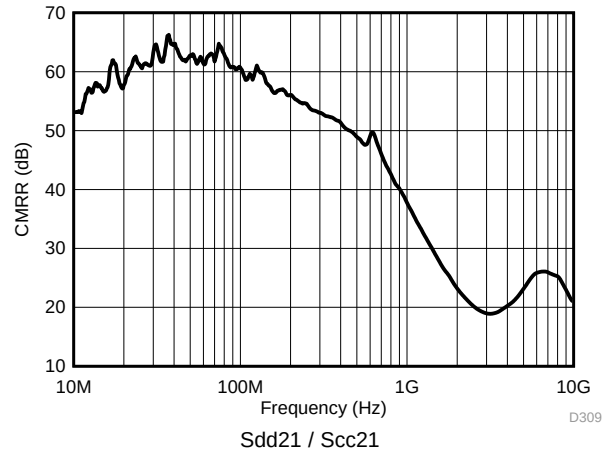
Single-ended input

Figure 46. S-Parameters



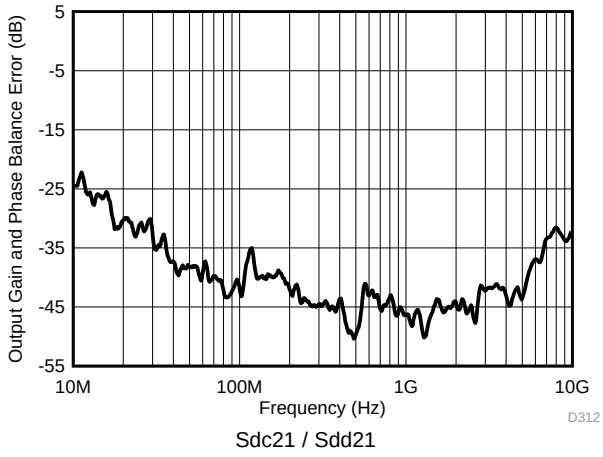
Scc21

Figure 47. Common-Mode Frequency Response



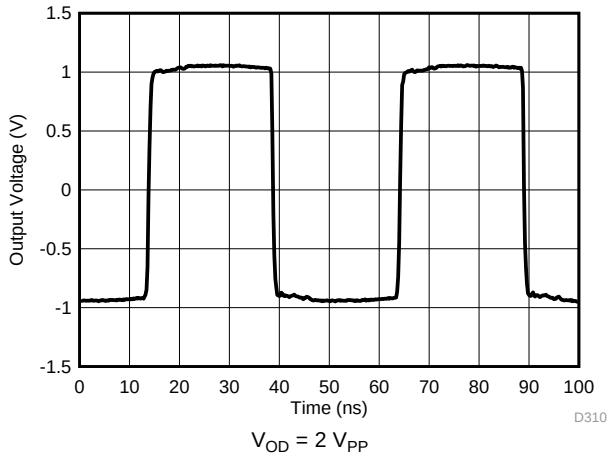
Sdd21 / Scc21

Figure 48. Common-Mode Rejection Ratio



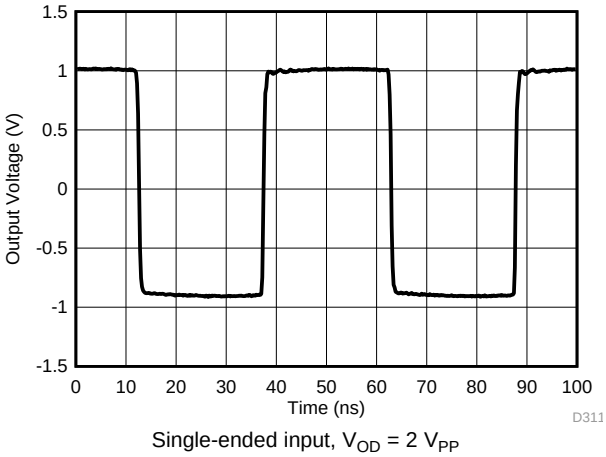
Sdc21 / Sdd21

Figure 49. Output Balance Error



V_{OD} = 2 V_{PP}

Figure 50. Pulse Response



Single-ended input, V_{OD} = 2 V_{PP}

Figure 51. Pulse Response

Typical Characteristics: V_S = 3.3 V (continued)

At T_A = 25°C, V_S = ±1.65 V, V_{CMx} = V_{CMA} or V_{CMB} = 0 V, R_L = 200-Ω differential, differential input and differential output, output measured at OUT_AMP reference point (see *Output Reference Points* section), and input and output pins referenced to midsupply (unless otherwise noted). Plot data measured using an EVM, as discussed in the *Parameter Measurement Information* section (see Figure 61 to Figure 63).

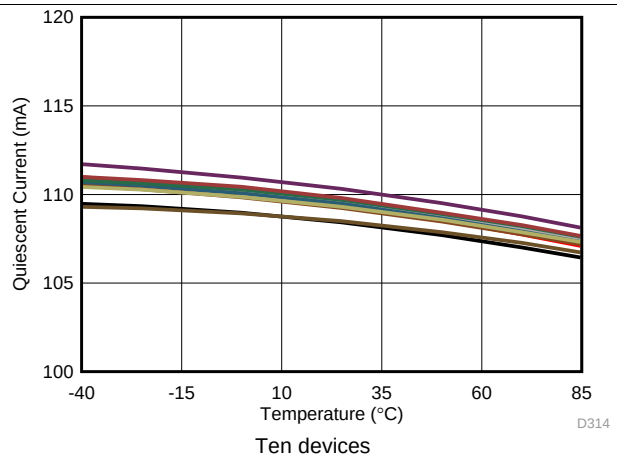


Figure 52. Quiescent Current vs Temperature

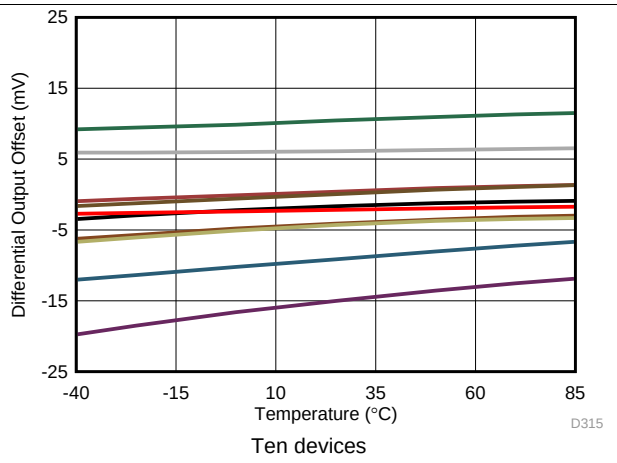


Figure 53. Differential Output Offset Votage vs Temperature

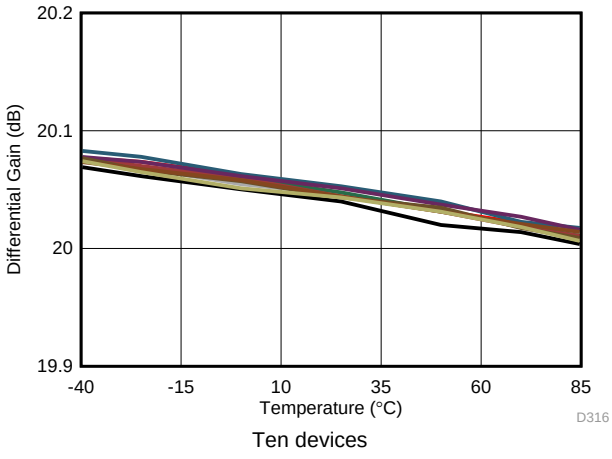


Figure 54. Differential Gain vs Temperature

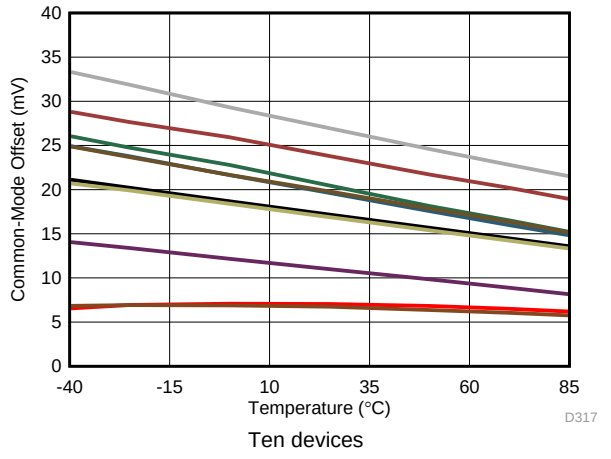


Figure 55. Common-Mode Offset Voltage vs Temperature

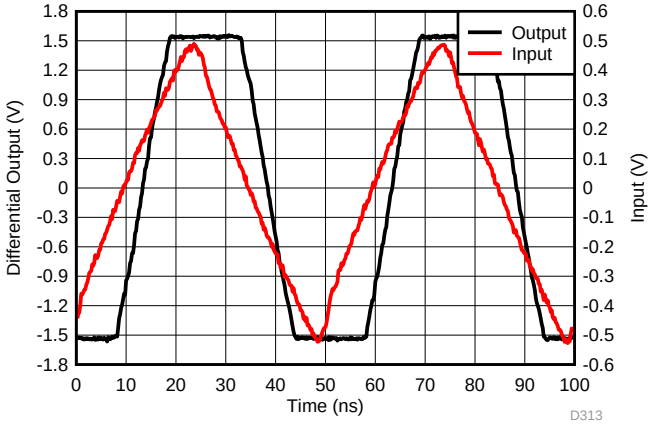
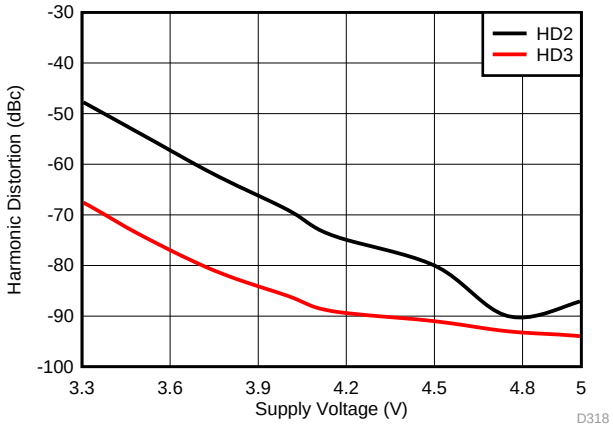


Figure 56. Overdrive Recovery

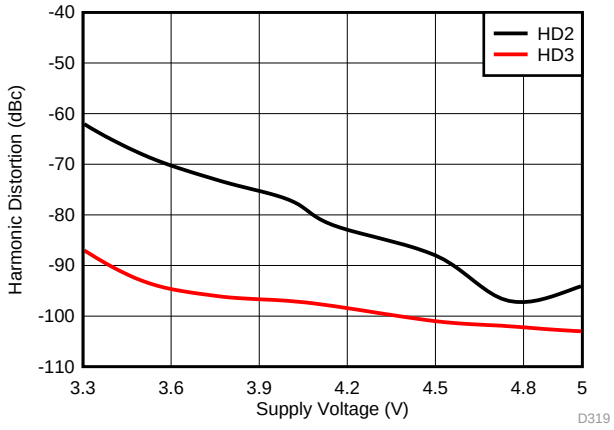
7.9 Typical Characteristics: V_S = 3.3 V to 5 V

At T_A = 25°C, V_{CMx} = V_{CMA} or V_{CMB} = 0 V, R_L = 200-Ω differential, differential input and differential output, output measured at OUT_AMP reference point (see *Output Reference Points* section), and input and output pins referenced to midsupply (unless otherwise noted). Plot data measured using an EVM, as discussed in the *Parameter Measurement Information* section (see Figure 61 to Figure 63).



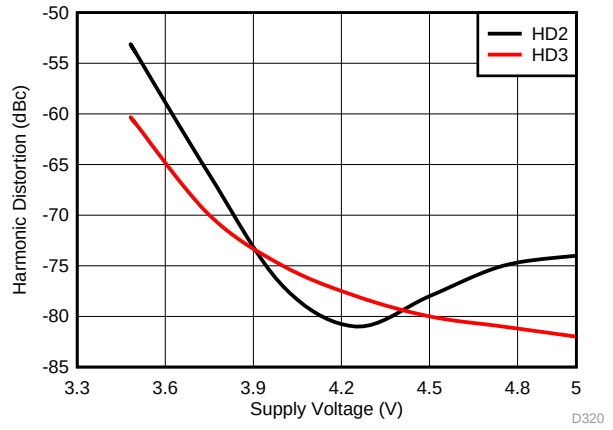
V_{OD} = 2 V_{PP}, f = 500 MHz

Figure 57. Harmonic Distortion vs Supply Voltage



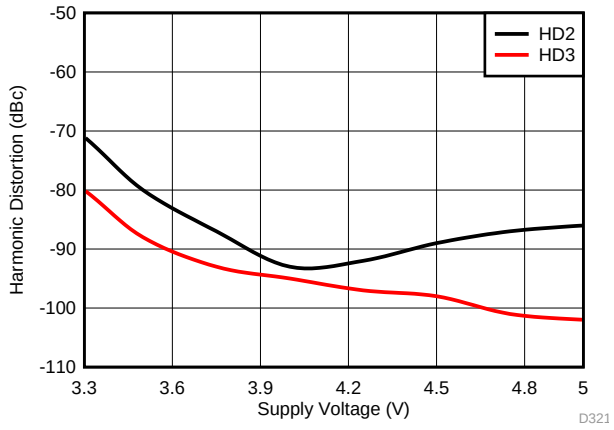
V_{OD} = 1 V_{PP}, f = 500 MHz

Figure 58. Harmonic Distortion vs Supply Voltage



Single-ended input, V_{OD} = 2 V_{PP}, f = 400 MHz

Figure 59. Harmonic Distortion vs Supply Voltage



Single-ended input, V_{OD} = 1 V_{PP}, f = 400 MHz

Figure 60. Harmonic Distortion vs Supply Voltage

8 Parameter Measurement Information

8.1 Output Reference Points

The LMH3404 is a fully differential amplifier (FDA) with fixed internal gain and feedback resistors for a signal gain of 20 dB (10 V/V). For most of this document, data were collected for both single-ended-to-differential (SE-Diff) and differential-to-differential (Diff-Diff) conversions in the diagrams illustrated in the *Test Circuits* section.

When matching the output to a 100-Ω load, the evaluation module (EVM) uses external 40-Ω resistors to complete the output matching. Using on-chip output resistors creates two potential reference points for measuring the output voltage. The amplifier output pins create one output reference point (OUT_AMP). The other output reference point is on the EVM at the matched 100-Ω load (OUT_LOAD). These points are illustrated in Figure 61 to Figure 63; see the *Test Circuits* section.

Most measurements in the *Electrical Characteristics* tables and in the *Typical Characteristics* sections are measured with reference to the OUT_AMP reference point. The conversion between reference points is a straightforward reduction of 3 dB for power and 6 dB for voltage, as shown in Equation 1 and Equation 2, respectively. The measurements are referenced to OUT_AMP when not specified.

$$POUT\_LOAD = (POUT\_AMP - 3\ dB) \quad (1)$$

$$VOUT\_LOAD = (VOUT\_AMP - 6\ dB) \quad (2)$$

8.2 ATE Testing and DC Measurements

All production-tested dc parameters are measured on automated test equipment. Measurements such as output-current sourcing and sinking are made in reference to the device output pins. Some measurements are referenced to the output of the internal amplifier, and do not include losses attributed to the on-chip output resistors. The *Electrical Characteristics* tables specify these conditions. When the measurement is referred to the amplifier output, then the output resistors are not included in the measurement. If the measurement is referred to the device pins, then the output resistor loss is included in the measurement.

8.3 Frequency Response

Frequency response is measured with both single-ended inputs and differential inputs.

For tests with single-ended inputs, the standard EVM is modified to include termination resistors on the amplifier inputs; see Figure 61. In order to provide a matched input, both inputs require external termination resistors to create a broadband, single-ended, 50-Ω match. Because the LMH3404 is fully symmetrical, either input (INA± or INB±) can be used for single-ended inputs, but both

IN*x* input pairs must be terminated properly. See the *Resistor Design Equations for Single-to-Differential Applications* section for more information on setting these resistors per gain and source impedance requirements.

When using a fully differential four-port network analyzer, neither input requires external termination; the network analyzer provides proper differential termination. Figure 62 illustrates a test circuit for differential input and output. To make frequency response measurements for either configuration, a network analyzer is connected to the input and output of the EVM with 50-Ω coaxial cables, and is set to measure the forward transfer function (s21). The input-signal frequency is swept, with the signal level set for the desired output amplitude.

8.4 Frequency Response (CMA and CMB Pins)

For the common-mode frequency response measurement, the standard EVM is used with the R_{CM+} and $R_{CM–}$ resistors removed, and a new resistor installed at R_{TCM} = 49.9 Ω. A network analyzer is connected to the CMA or CMB input of the EVM, and the EVM outputs are connected to the network analyzer with 50-Ω coaxial cables. The network analyzer is set to single-ended input and differential output configuration, and the output common-mode is measured with respect to the single-ended input (Scs21). The input signal frequency is swept with the signal level set for 100 mV (–16 dBm). The common-mode control circuit gain is one.

8.5 S-Parameters

The standard EVM is used for all S-parameter measurements. All four ports are used, or are terminated with 50-Ω connections; see the *Frequency Response* section for more information.

8.6 Distortion

The standard EVM is used for measuring single-tone harmonic distortion and two-tone intermodulation distortion. Distortion is measured with both differential and single-ended input signals; see Figure 62 and Figure 61. In order to differentially interface with single-ended test equipment, baluns are required between the amplifier output ports and the test equipment. These baluns are used to combine two tones in the two-tone test plots. For single-ended distortion measurements, the same termination must be used on both input pins. When a filter is used on the driven input port, the same filter and a broadband load are used to terminate the other input. When the signal source is a broadband controlled impedance, then only a broadband-controlled impedance is required to terminate the unused input. The LMH3404EVM uses a series inductor on the power supply that is tuned to optimize wideband distortion performance, but can be changed for narrowband applications. See the second paragraph of the *Supply Decoupling* section for more information.

8.7 Noise Figure

For noise figure measurement, the standard EVM is used with a differential input matched to a 100-Ω and a differential output.

8.8 Pulse Response, Slew Rate, and Overdrive Recovery

The standard EVM is used for time-domain measurements. The input is single-ended with the differential outputs routed directly to the oscilloscope inputs. The differential signal response is calculated from the two separate oscilloscope inputs. In addition, the common-mode pulse response is also captured in this configuration.

8.9 Power-Down Mode

The standard EVM is used to power down the device, with the shorting block on jumper JENA and JENB removed completely. A high-speed, 50-Ω pulse generator is used to drive the enable pins (ENA and ENB), and the output signal is measured with an input stimulus present (such as a 250-MHz, sine-wave input).

8.10 Crosstalk

For crosstalk measurement, the standard EVM is used with both channels enabled; channel A is driven differentially with a single tone source, and no input is presented to channel B. A spectrum analyzer is used to measure the output of channel B at the frequency of the channel-A input signal.

8.11 Test Circuits

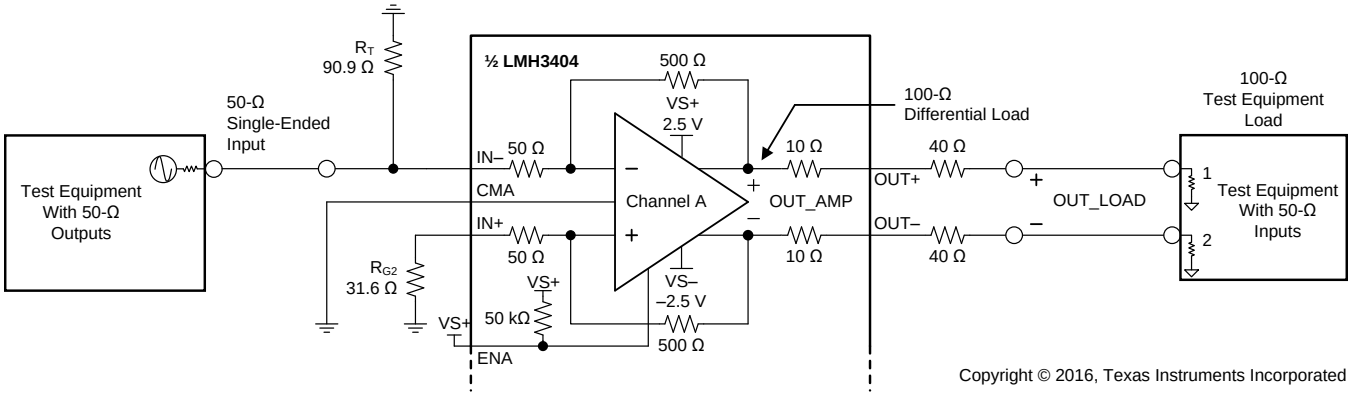


Figure 61. Test Circuit: Single-Ended Input, Differential Output

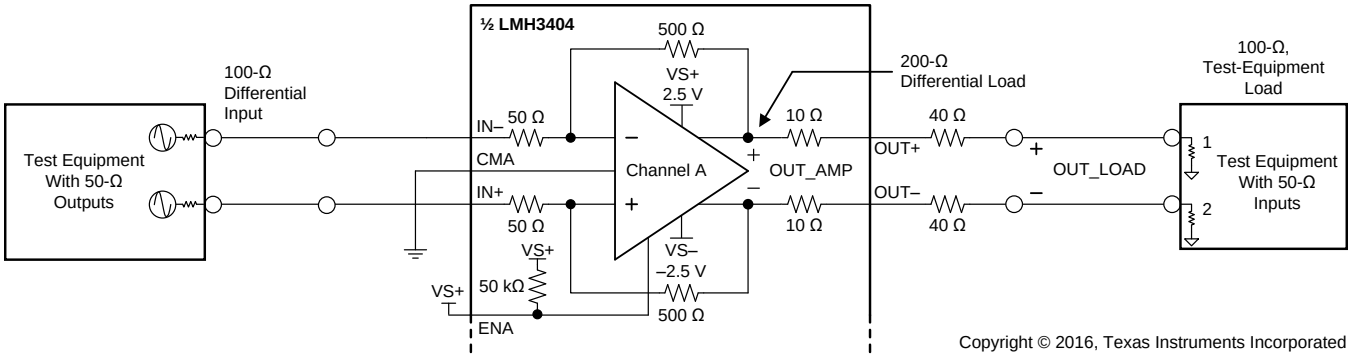


Figure 62. Test Circuit: Differential Input, Differential Output

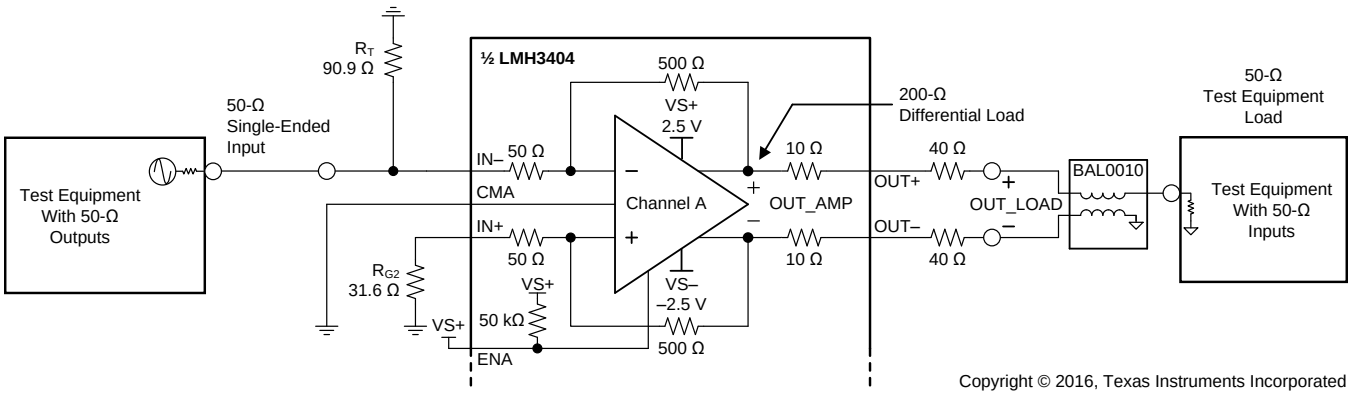


Figure 63. Test Circuit: Single-Ended Harmonic Distortion

9 Detailed Description

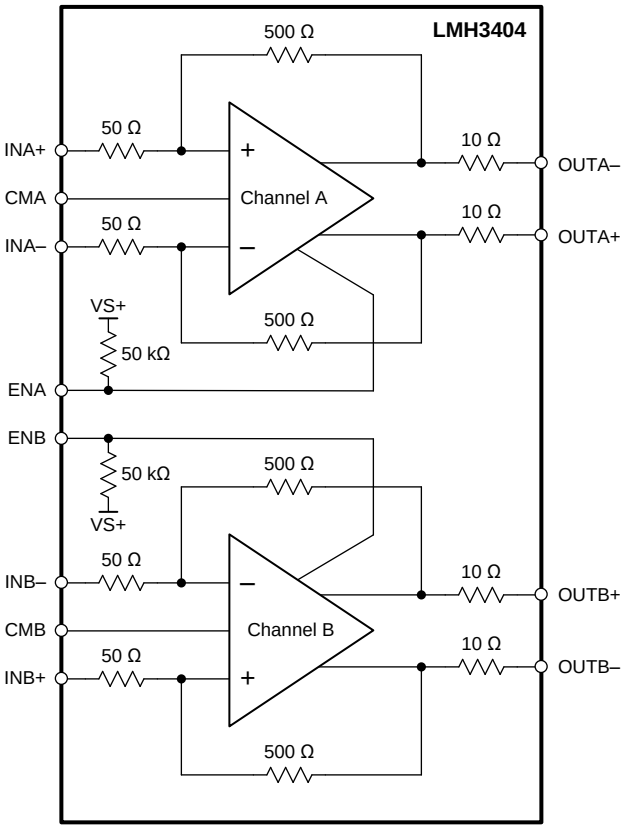
9.1 Overview

The LMH3404 is a very high-performance, dual-channel, differential amplifier with a gain bandwidth product (GBP) equal to 7 GHz. The LMH3404 is optimized for radio frequency (RF) and intermediate frequency (IF) or high-speed, time-domain, wide-bandwidth applications. The device is also ideal for dc- or ac-coupled applications that may require a single-ended-to-differential (SE-Diff) conversion when driving an analog-to-digital converter (ADC). The feedback (R_F) and gain set (R_G) resistors are internal to the device, and are set for a gain of 20 dB (10 V/V).

A common-mode reference input pin is provided to align the amplifier output common-mode with the ADC input requirements. Power supplies between 3.15 V and 5.25 V can be used, and dual-supply operation is supported. A power-down feature is also available for power savings.

The LMH3404 offers two on-chip termination resistors, one for each output with values of 10 Ω each. For most load conditions, the 10-Ω resistors are only a partial termination. Consequently, external termination resistors are required for most applications. See Table 2 for some common load values and matching resistors.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Fully Differential Amplifier

The LMH3404 is a dual-channel, voltage-feedback, fully differential amplifier (FDA) offering a small-signal bandwidth (SSBW) of 7 GHz, with an internally-fixed gain of 20 dB. The core differential amplifiers are voltage-feedback designs with high slew rate and excellent linearity of up to 2 GHz.

The output average voltage (common-mode) is controlled by a separate common-mode loop. The target for this output average is set by the CMA and CMB input pins. The output common-mode voltage (V_{OCM}) range extends from 1.1 V below the midsupply voltage to 1.1 V above the midsupply voltage, when using a total 5-V supply. On a 3.3-V supply, the output common-mode range is quite small. For applications using a 3.3-V supply voltage, the output common-mode voltage must remain very close to the midsupply voltage.

The input common-mode voltage offers more flexibility than the output common-mode voltage. The input common-mode voltage range extends from the negative rail to approximately 1 V above the midsupply voltage, when powered with a 5-V supply.

Two enable pins are included: ENA and ENB. These pins are referenced to the thermal pad (typically, ground) with a nominal switching threshold voltage of 1 V. Set an enable pin voltage to less than the specified minimum voltage to turn the device off, and place the LMH3404 into a very-low quiescent current state. When disabled, the signal path is still present through the passive external resistors. Input signals applied to a disabled LMH3404 device still appear at the outputs at some level through this passive resistor path, as with any disabled FDA device. The enable pins are biased to a logic-low state with a 50-kΩ internal resistor.

9.3.2 Single-Ended to Differential Signal Operation

One of the most useful features supported by the FDA device is an easy conversion from a single-ended input to a differential output centered on a user-controlled, common-mode voltage level. Although the output side is relatively straightforward, the device input pin common-mode voltage level moves relative to both the input signal common-mode voltage and output common-mode voltage. This feature acts to increase the apparent input impedance to be greater than the R_G value. However, this feature causes input clipping if this common-mode signal moves beyond the input range. This input active impedance issue applies to both ac- and dc-coupled designs, and requires somewhat more complex solutions for the resistors to account for this active impedance, as described in this section.

9.3.2.1 AC-Coupled Signal Path Considerations for Single-Ended Input to Differential Output Conversion

When the signal path is ac coupled, the dc biasing for the LMH3404 becomes a relatively simple task. In all designs, start by defining the output common-mode voltage. The ac-coupling issue can be separated for the input and output sides of an FDA design. The input can be ac coupled and the output dc coupled, or the output can be ac coupled and the input dc coupled, or they can both be ac coupled.

One situation where the output can be dc coupled (for an ac-coupled input), is when driving directly into an ADC where the V_{OCM} control voltage uses the ADC common-mode reference to directly bias the FDA output common-mode voltage to the required ADC input common-mode voltage. The common-mode feedback path must always be dc coupled in any configuration. In any case, the design starts by setting the desired V_{OCM}. When an ac-coupled path follows the output pins, the best linearity is achieved by operating V_{OCM} at midsupply. The V_{OCM} voltage must be within the linear range for the common-mode loop, as specified in the output voltage parameters of the *Electrical Characteristics*. To limit noise, place a 0.1-µF decoupling capacitor on each V_{OCM} pin to ground. The CMA and CMB pins must be connected to a reference voltage because these pins do not have any internal biasing.

After V_{OCM} is defined, check the target output voltage swing to make sure that the V_{OCM} positive or negative output swing on each side does not clip into the supplies. If the desired output differential swing is defined as V_{OPP}, divide by four to obtain the positive or negative voltage swing around V_{OCM} at each of the two output pin pairs (each pin pair operates 180° out-of-phase with the other). Check that $\pm V_{OCM}$ voltage does not exceed the output swing of this device. Going to the device-input-pins side (because both the source and balancing resistor on the nonsignal-input-side are dc blocked; see Figure 65), no common-mode current flows from the output

Feature Description (continued)

common-mode voltage, thus setting the input common-mode voltage to be equal to the output common-mode voltage. This input headroom also sets a limit for higher V_{OCM} voltages. The minimum headroom for the input pins to the positive supply overrides the headroom limit for V_{OCM} output because the input common-mode voltage (V_{ICM}) is V_{OCM} for ac-coupled sources. Also, the input signal moves V_{ICM} around the dc bias point, as described in the *Resistor Design Equations for Single-to-Differential Applications* section.

9.3.2.2 DC-Coupled Input Signal Path Considerations for SE-Diff Conversions

For dc-coupled configurations, the output considerations remain the same as for the ac-coupled design. Again, the input can be dc-coupled when the output is ac-coupled. A dc-coupled input with an ac-coupled output has some advantages; for example, to move the input V_{ICM} down if the source is ground referenced. When the source is dc-coupled into the LMH3404 (as shown in Figure 64), both sides of the input circuit must be dc coupled to retain differential balance. Normally, the non-signal input side is biased to whatever the source midrange is expected to be. Providing this midscale reference gives a balanced differential swing around V_{OCM} at the outputs.

Often, the nonsignal input is simply grounded for dc-coupled, bipolar-input applications. This configuration gives a balanced differential output if the source swings around ground. If the source swings from ground to some positive voltage, grounding the nonsignal input gives a unipolar output differential swing from both outputs at V_{OCM} (when the input is at ground) to one polarity of swing. Biasing the nonsignal input to an expected midpoint for the input signal creates a differential output swing around V_{OCM}. One significant consideration for a dc-coupled input is that if V_{OCM} and V_{ICM} are not equal, then a common-mode bias current is present from the output through R_F and R_G to the source on both sides of the feedback. The source must then be able sink or source this dc current.

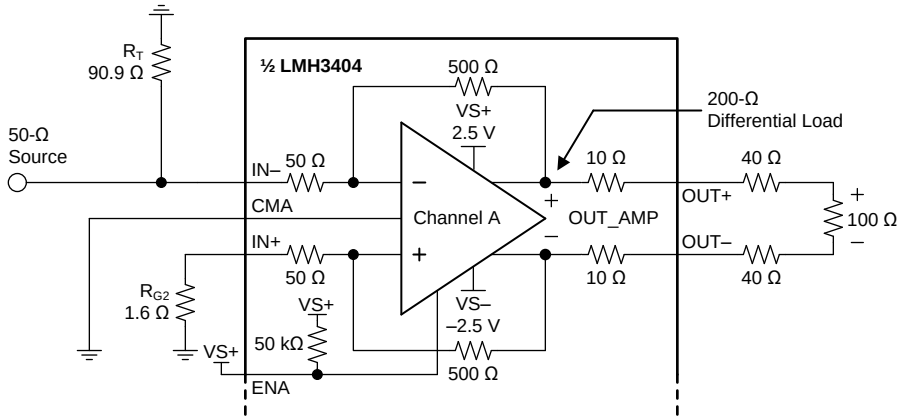


Figure 64. DC-Coupled, Single-Ended-to-Differential Configuration

9.3.2.3 Resistor Design Equations for Single-to-Differential Applications

Even though LMH3404 gain is configured through internal resistors, being familiar with the FDA resistor selection criteria is still important. The design equations for setting the resistors around an FDA to convert from a single-ended input signal to a differential output can be approached in several ways. For the purposes of this derivation, the amplifier is treated as if the feedback is externally set in order to make the solution applicable for all types of fully differential amplifiers. In the case of the LMH3404, the feedback and gain resistor values in the equations are simply set to the internal values of the LMH3404 feedback resistors. To derive the design equations and simplify the results, follow these guidelines:

- Select the feedback resistors first
- Set the feedback resistors to be equal on the two sides of the device; not an issue for the LMH3404 because the feedback resistors are internal.
- Set the dc and ac impedances from the summing junctions back to the signal source and ground (or a bias voltage on the nonsignal input side) to be equal in order to retain the feedback divider balance on each side of the FDA.

Feature Description (continued)

These guidelines are typical and are aimed to deliver the best dynamic range through the FDA signal path. Most FDA amplifiers use external resistors and have complete flexibility in the selected R_F; however. the LMH3404 has on-chip feedback resistors that are fixed at 500 Ω. When computing a solution for the LMH3404, the value of R_F used in the equations in this section must always be set to 500 Ω . Similarly, the LMH3404 also has internal gain resistors set at 50 Ω. For the variables in the equations, the value of R_{G1} must be set to 50 Ω, and R_{G2} becomes the value of an external resistor added to the nonsignal pin plus the internal 50 Ω.

After the feedback resistor values are chosen, the aim is to solve for R_T (a termination resistor to ground on the signal input side) and R_{G2} (the matching gain resistor on the nonsignal input side) that yield the correct value of 50 Ω for R_{G1} (the input gain resistor for the signal path); see Figure 65. The same resistor solutions can be applied to either ac- or dc-coupled paths. Adding blocking capacitors in the input-signal chain is a simple option. Adding these blocking capacitors after the R_T element (see Figure 65) has the advantage of removing any dc currents in the feedback path from the output V_{OCM} to ground.

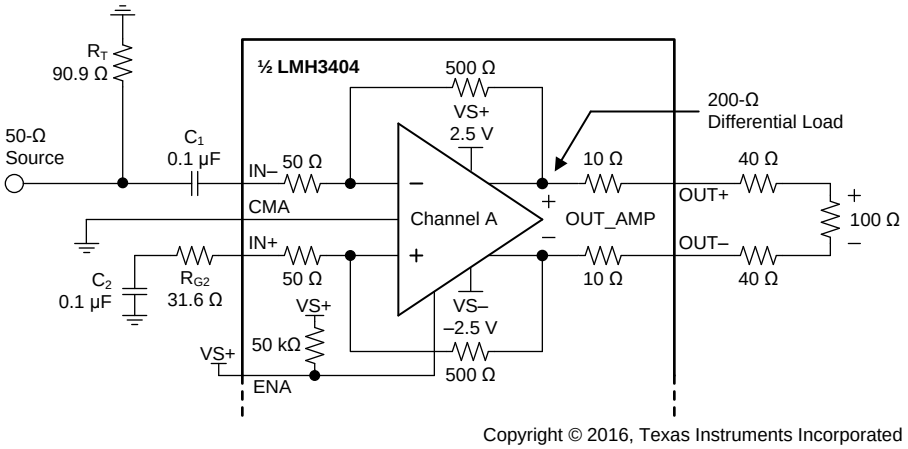


Figure 65. AC-Coupled, Single-Ended Source Configuration

With a predetermined value for R_{G1}, it is easiest to follow an iterative approach to find the required R_T and R_{G2}. Using Equation 3, solve for the value of RT for different chosen gains. The only inputs required are:

1. The selected R_F value.
2. The target voltage gain (A_V) from the input of R_T to the differential output voltage.
3. The desired input impedance at the junction of R_T and R_{G1} to match the source resistance, R_S.

Solving this quadratic for R_T starts the solution sequence, as shown in Equation 3:

$$R_T^2 - R_T \frac{2R_S\left(2R_F + \frac{R_S}{2}A_V^2\right)}{2R_F\left(2+A_V\right) - R_S A_V(4+A_V)} - \frac{2R_F R_S^2 A_V}{2R_F\left(2+A_V\right) - R_S A_V(4+A_V)} = 0 \quad (3)$$

For a quadratic, there are limits to the range of solutions. Specifically, after R_F and R_S are chosen, there is a maximum gain, beyond which Equation 3 starts to solve for negative R_T values (if input matching is a requirement). With R_F selected, use Equation 4 to verify that the maximum gain is greater than the desired gain.

$$Av_{max} = \left(\frac{R_F}{R_S} - 2\right) \bullet \left[1 + \sqrt{1 + \frac{4\frac{R_F}{R_S}}{\left(\frac{R_F}{R_S} - 2\right)^2}}\right] \quad (4)$$

Feature Description (continued)

If the achievable A_{Vmax} is less than desired, increase the R_F value. After R_T is derived from Equation 3, the R_{G1} element is given by Equation 5:

$$R_{G1} = \frac{2\frac{R_F}{A_V} - R_S}{1 + \frac{R_S}{R_T}} \tag{5}$$

From this point, the process can be iterated starting from Equation 3 with an adjusted value for A_V, until a value close to 50 Ω is reached for R_{G1}. Then, the simplest approach is to use a single $R_{G2} = R_T \parallel R_S + R_{G1}$ on the nonsignal input side. Often, this approach is shown as the separate R_{G1} and R_S elements. This approach can provide a better divider match on the two feedback paths, but a single R_{G2} is often acceptable. A direct solution for R_{G2} is given as Equation 6:

$$R_{G2} = \frac{2\frac{R_F}{A_V}}{1 + \frac{R_S}{R_T}} \tag{6}$$

It is important to remember in this case that R_{G2} is the value of the internal 50-Ω resistor plus added external resistance to balance the amplifier. This design proceeds from a target input impedance matched to R_S, signal gain A_V, and a selected R_F value. As discussed previously, this resistance is on-chip, and therefore the R_F value cannot be changed. Refer to Figure 61 in the *Test Circuits* section that shows the value of resistors used for characterization in this document.

9.3.2.4 Input Impedance Calculations

The designs so far have included a source impedance, R_S, that must be matched by R_T and R_{G1}. The total impedance with respect to the input at R_{G1} for the circuit of Figure 64 is the parallel combination of R_T to ground and ZA (active impedance) presented by the amplifier input at R_{G1}. Assuming R_{G2} is set to obtain a differential divider balance, that expression is given by Equation 7:

$$ZA = R_{G1}\frac{\left(1 + \frac{R_{G1}}{R_{G2}}\right)\left(1 + \frac{R_F}{R_{G1}}\right)}{2 + \frac{R_F}{R_{G2}}} \tag{7}$$

For designs that do not need impedance matching (but instead come from the low-impedance output of another amplifier, for instance), $R_{G1} = R_{G2}$ is the single-to-differential design used without R_T to ground. Setting $R_{G1} = R_{G2} = R_G$ in Equation 7 gives the input impedance of a simple input FDA driving from a low-impedance, single-ended source to a differential output. For the LMH3404 typically, R_{G1} is set to 50 Ω to match the internal resistor, and R_{G2} is the value of the other nonsignal input internal 50-Ω resistor plus an external resistance determined from Equation 6.

9.3.3 Differential-to-Differential Operation

The LMH3404 can also be used to amplify differential input signals to differential output signals. In many ways, this method is a much simpler way to operate the FDA from a design equations perspective. Again, because the two sides of the circuit are balanced internally with equal R_F and R_G elements, the differential input impedance is now just the sum of the two R_G elements to a differential, inverting summing junction. In these designs, the input common-mode voltage at the summing junctions does not move with the signal, but must be dc-biased in the allowable range for the input pins, with consideration given to the voltage headroom required to each supply. Slightly different considerations apply to ac- or dc-coupled, differential-in to differential-out designs, as described in the following subsections.

Feature Description (continued)

9.3.3.1 AC-Coupled, Differential-Input to Differential-Output Design Issues

When using the LMH3404 with an ac-coupled differential source, the input can be coupled through two blocking capacitors. An optional input differential termination resistor (R_M) can be included to change the effective input impedance of the amplifier to match different source impedances. In Figure 66, the R_G elements sum to show a 100-Ω differential impedance, and the R_M element combines in parallel, to give a net 50-Ω, ac, differential impedance to the source. The design proceeds ideally by selecting an R_M element that achieves a target input impedance with a value different than the 100-Ω differential impedance presented by the internal R_G resistors. The dc biasing in Figure 66 is very simple. The output V_{OCM} is set by the input control voltage, and because there is no dc current path for the output common-mode voltage, that dc bias also sets the input pins common-mode operating points.

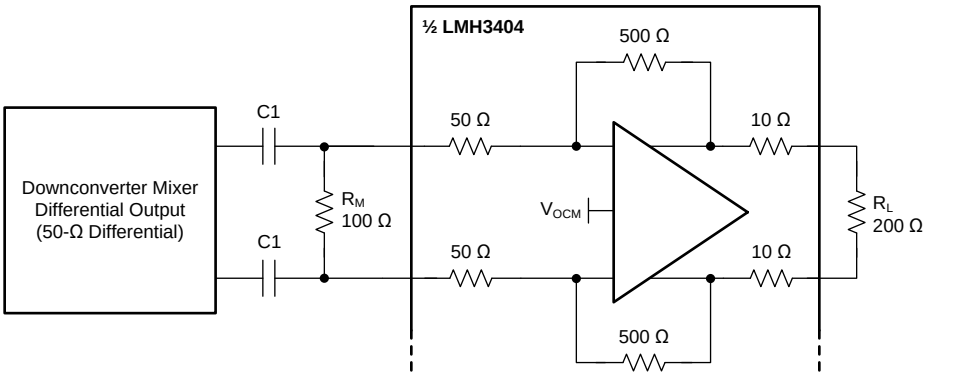


Figure 66. Downconverting Mixer AC Coupled to the LMH3404

9.3.3.2 DC-Coupled, Differential-Input to Differential-Output Design Issues

Operating the LMH3404 with a dc-coupled input source simply requires that the input pins stay in range of the dc common-mode operating voltage. Only a differential termination resistor R_M may be required to match a desired source impedance.

9.3.4 Output Common-Mode Voltage

The CMA and CMB input pin voltages control the output common-mode voltage. The CMA and CMB pins have no internal biasing network and must be driven by an external source or resistor divider network to the positive power supply. The CMA and CMB input impedances are very high, and bias current is not critical. It is also necessary to use a bypass capacitor; a capacitor value of 0.01 µF is recommended. For best harmonic distortion, maintain the CMA and CMB input pin voltages within ±1 V of the midsupply voltage when using a 5-V supply, and within ±0.5 V when using a 3.3-V supply. The CMA and CMB input pin voltages can be operated outside this range if a lower output swing is used, or if distortion degradation is allowed.

9.4 Device Functional Modes

9.4.1 Operation With a Split Supply

The LMH3404 can be operated using split supplies. One of the most common supply configurations is ±2.5 V. In this case, VS+ is connected to 2.5 V, VS– is connected to –2.5 V, and the thermal pad is connected to the system ground. As with any device, the LMH3404 allowable pin voltages are all relative. In essence, using split supplies is simply a level shift of the power pins by –2.5 V. If everything else is level-shifted by the same amount, the device does not detect any difference. With a ±2.5-V power supply, the output common-mode range is 0 V ±1 V; the input has a slightly larger range of –2.5 V to 1 V. This design has certain advantages in systems where signals are referenced to ground, and for driving ADCs with low input common-mode voltage requirements in dc-coupled applications, as noted in the *ADC Input Common-Mode Voltage Considerations: DC-Coupled Input* section. With the GND pin connected to the system ground, the enable threshold is 1.2 V, which is compatible with most logic levels from 1.5-V CMOS to 2.5-V CMOS.

As noted previously, the absolute supply voltage values are not critical. For example, using a 4-V VS+ and a –1-V VS– still results in a 5-V supply condition. As long as the input and output common-mode voltages remain in the optimum range, the amplifier can operate on any supply voltages from 3.3 V to 5.25 V. When considering using supply voltages near the 3.3-V total supply, be very careful to make sure that the amplifier performance is adequate. Setting appropriate common-mode voltages for large-signal swing conditions becomes difficult when the supply voltage is below 4 V.

9.4.2 Operation With a Single Supply

As with split supplies, the LMH3404 can be operated from single-supply voltages from 3.3 V to 5.25 V. Single-supply operation is most appropriate when the signal path is ac-coupled and the input and output common-mode voltages are set to midsupply by the CMA and CMB pins, and are preserved by coupling capacitors on the input and output.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Stability

Two types of gain are associated with amplifiers: noise and signal gain. Noise gain (NG) is what is used to best determine the stability of an amplifier. The noise gain is the inverse of the voltage divider from the outputs back to the differential inputs. This gain is calculated by NG = (R_F / R_{IN}) + 1, where R_{IN} = R_G + R_S. For the LMH3404, the internal resistors are designed to keep the device stable when matched to a 100-Ω differential load. If the noise gain is decreased by adding more source resistance (R_S) then the device eventually becomes unstable. If low gain stability is needed, the noise gain can be altered with the addition of a *dummy* resistor (R_T in the differential configuration of Figure 67). By manipulating the noise gain with this addition, the amplifier can be stabilized without affecting signal gain. In Figure 67, R_S and R_T in parallel combination become the effective value for R_S, and can increase noise gain of the amplifier by choosing R_T wisely. R_G and R_F are the main gain-setting resistors and the addition of R_T adjusts the noise gain for stability. Much of this stability can be simulated using the LMH3404 TINA model, depending on the amplifier configuration. The example in Figure 67 uses the LMH3404, a signal gain from the differential inputs to differential outputs of 2.5 V/V, and a noise gain of 6 V/V.

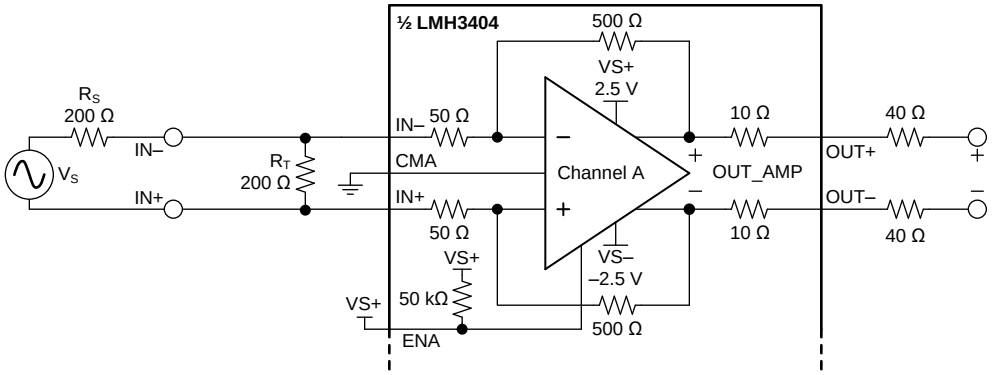


Figure 67. Differential Stability

10.1.2 Input and Output Headroom Considerations

The starting point for most designs is to assign an output common-mode voltage. For ac-coupled signal paths, this starting point is often the default midsupply voltage. This configuration retains the most available output swing around the output operating point, which should be centered with V_{OCM} equal to the midsupply point. For dc-coupled designs, set this voltage with consideration for the required minimum headroom to the supplies listed in the *Electrical Characteristics* tables for output common-mode voltage control. From that target output V_{OCM}, the next step is to verify that the desired output differential V_{PP} stays within the supplies. For any desired differential output voltage (V_{OPP}) check the maximum possible signal swing for each output pin. Make sure that each pin can swing to the voltage required by the application.

For instance, when driving the ADC12D1800RF with a 1.25-V common-mode voltage and 0.8-V_{PP} input swing, the maximum output swing is set by the negative-going signal from 1.25 V to 0.2 V. The negative swing of the signal is directly at the edge of the output swing capability of the LMH3404. In order to set the output common-mode voltage to an acceptable range, use a negative power supply of at least –1 V. The ideal negative supply voltage is the ADC V_{CM} – 2.5 V for the negative supply, and the ADC V_{CM} + 2.5 V for the input swing. In order to use the existing supply rails, deviating from the ideal voltage may be necessary.

Application Information (continued)

With the output headroom confirmed, the input junctions must also stay within their operating range. The input range extends nearly to the negative supply voltage; therefore, input range limitations only appear when approaching the positive supply where a maximum 1.3-V headroom is required.

The input pins operate at voltages set by the external circuit design, the required output V_{OCM}, and the input signal characteristics. With a differential input, the input pins operate at a fixed input V_{ICM}, and the differential input signal does not influence this common-mode operating voltage. AC-coupled differential input designs have a V_{ICM} equal to the output V_{OCM}. DC-coupled differential input designs must check the voltage divider from the source V_{CM} to the LMH3404 CM setting. That result solves to an input V_{ICM} within the specified range. If the source V_{CM} can vary over some voltage range, the headroom calculations must include this variation.

10.1.3 Noise Analysis

The LMH3404 has an internal fixed gain; therefore, the input voltage and current specifications cannot be directly measured. The internal amplifier inputs after the gain resistors are not accessible. In order to present a similar specification, the noise of the LMH3404 is listed as an input voltage noise referred to the device inputs. To obtain this value, the measured output voltage noise of the device is divided by the voltage gain of the device referenced to the input (A_V). However, to aid in circuit design and analysis, a simulated internal amplifier input voltage and current noise of 1.25 nV/√Hz and 3.5 pA/√Hz have been provided in the *Electrical Characteristics* table. These values can be used in a standard output noise analysis in order to compute the noise impact of additional input series resistors in the circuit.

The first step in the output noise analysis is to reduce the application circuit to its simplest form with equal feedback and gain setting elements to ground, shown in Figure 68) with the FDA and resistor noise terms to be considered. For the LMH3404, the values of the resistors are internally set; however if series resistance is added to the inputs, this series resistance adds to the internal 50-Ω R_G resistor to form a new effective R_G.

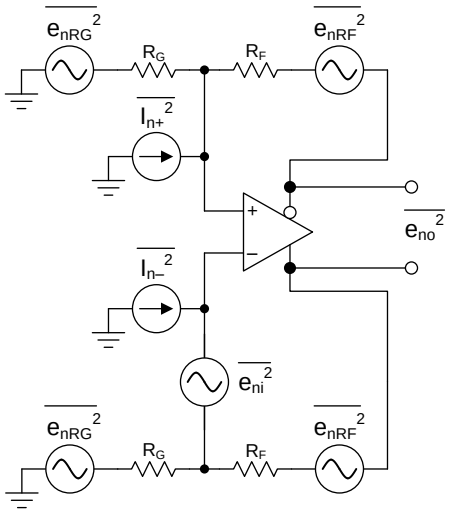


Figure 68. FDA Noise-Analysis Circuit

Application Information (continued)

The noise powers are shown in Figure 68 for each term. When the R_F and R_G terms are matched on each side, the total differential output noise is the root sum of squares (RSS) of these separate terms. Using NG (noise gain) ≡ 1 + R_F / R_G, the total output noise (e_{no}) is given by Equation 8. Each resistor noise term is a 4kTR power.

$$e_{no} = \sqrt{(e_{ni}NG)^2 + 2(i_nR_F)^2 + 2(4kTR_FNG)} \quad (8)$$

where

- The first term is simply the internal, differential-input spot noise times the noise gain.
- The second term is the internal input current noise terms times the feedback resistor (and because there are two terms, the power is two times one of the terms).
- The last term is the output noise resulting from both the R_F and R_G resistors, again times two, for the output noise power of each side added together.

Using the exact values for a 100-Ω, matched, differential-to-differential gain sweep with a fixed R_F = 500 Ω, internal voltage noise e_{ni} = 1.25 nV/√Hz, and current noise i_n = 3.5 pA/√Hz for the LMH3404, gives an output spot noise from Equation 8. Then, dividing by the signal gain set through internal resistors (A_V), gives the input-pin-referred, spot-noise voltage (e_n) of 1.3 nV/√Hz. For the LMH3404, the current noise is an insignificant noise contributor because of the low value of R_F. When matching to a 100-Ω system, the R_G value in the NG equation becomes the combination of the internal 50-Ω resistor and half of the 100-Ω differential source resistance, to equal 100 Ω for the calculation. If the source resistance is not accounted for, the equation results in a higher value for the noise calculation.

If any series resistance is added to the input pins of the amplifier, the series resistance also affects the total noise of the amplifier. Table 1 shows the output noise effect of various series resistors added to the inputs of the amplifier. Added series resistance has the benefit of lowering the signal gain and total noise of the amplifier; however, too much added series resistance eventually makes the amplifier unstable.

Table 1. Output Noise With Various Added Series input Resistance

SOURCE RESISTANCE (Ω)	ADDED SERIES INPUT RESISTOR PER INPUT (Ω)	EFFECTIVE R_G (Ω)	NOISE GAIN (V/V)	OUTPUT NOISE e_{no} (nV/√Hz)
100	0	100	6	12.7
100	10	110	5.55	12.1
100	15	115	5.35	11.8
100	25	125	5	11.3

10.1.4 Noise Figure

Noise figure (NF) is a helpful measurement in a radio-frequency (RF) system design. The basis of this calculation is to define how much thermal noise the system (or even on the component) adds to this input signal. All systems are assumed to have a starting thermal noise power of –174 dBm/√Hz at room temperature, calculated from Equation 9:

$$P_{(dBW)} = 10 \times \log (kTB) \quad (9)$$

where

- T = temperature in kelvins = 290 K
- B = bandwidth in Hertz = 1 Hz
- k = Boltzmann's constant = 1.38 × 10^{-23} J/K

Whenever an element is placed in a system, additional noise is added beyond the thermal noise floor. The noise factor (F) helps calculate the noise figure, and is the ratio between the input signal-to-noise ratio (SNR) and the output SNR. Input SNR includes the noise contribution from the resistive part of the source impedance, Z_S. The NF measurement is relative to the source impedance used in the measurement or calculation because ideal capacitors and inductors are known to be noiseless. The NF measurement is calculated by Equation 10:

$$NF = 10 \log (e_{no}^2 / en_{Zs})$$

where

- $e_{n(Zs)}$ = the thermal noise of the source resistance = $4\ kTR_S\ (A_V D_T)^2$
- A_V is the voltage gain of the amplifier
- $D_T = 2R_G / (R_S + 2R_G)$ (10)

Using Equation 10 in conjunction with the measured output noise of 13.3 nV/$\sqrt{Hz}$ at 500 MHz, the NF is roughly equal to 6.5 dB. This value is slightly lower than the actual value of 6.6 dB measured on the bench at 500 MHz with a 100-Ω source resistance.

For thermal noise calculations with different source resistances, use Equation 10 to recalculate the NF referred to any source resistance. However, the output voltage noise (e_{no}) must also be recalculated in reference to the new source resistance in order to obtain the correct noise figure.

10.1.5 Thermal Considerations

The LMH3404 is packaged in a space-saving VQFN package with a thermal coefficient ($R_{\theta JA}$) of 54.5 °C/W. Limit the total power dissipation in order to keep the device junction temperature below 150°C for instantaneous power, and below 125°C for continuous power.

10.1.6 SNR Considerations

The signal-to-noise ratio (SNR) of the amplifier and filter is calculated from the amplitude of the signal and the bandwidth of the filter. The noise from the amplifier is band-limited by the filter with the equivalent brick-wall filter bandwidth. The amplifier and filter noise are calculated using Equation 11:

$$SNR_{AMP+FILTER} = 10 \times \log \left(\frac{V^2_O}{e^2_{FILTEROUT}} \right) = 20 \times \log \left(\frac{V_O}{e_{FILTEROUT}} \right)$$

where:

- $e_{FILTEROUT} = e_{NAMPOUT} \times \sqrt{ENB}$
- $e_{NAMPOUT}$ = the output noise density of the LMH3404 (13 nV/$\sqrt{Hz}$ at 100 MHz)
- ENB = the brick-wall equivalent noise bandwidth of the filter
- V_O = the amplifier output signal (11)

For example, with a first-order (N = 1) band-pass or low-pass filter with a 30-MHz cutoff, the ENB is $1.57 \times f_{-3dB}$ = 1.57 × 30 MHz = 47.1 MHz. For second-order (N = 2) filters, the ENB is $1.22 \times f_{-3dB}$. When filter order increases, the ENB approaches f_{-3dB} (N = 3 → ENB = $1.15 \times f_{-3dB}$; N = 4 → ENB = $1.13 \times f_{-3dB}$). Both V_O and $e_{FILTEROUT}$ are in RMS voltages. For example, with a 2-V_{PP} (0.707 V_{RMS}) output signal and a 100-MHz first-order filter, the SNR of the amplifier and filter is 72.8 dB with $e_{FILTEROUT}$ = 13 nV/$\sqrt{Hz}$ × $\sqrt{157\ MHz}$ = 163 μV_{RMS}.

The SNR of the amplifier, filter, and ADC sum in RMS fashion is as shown in Equation 12 (SNR values in dB):

$$SNR_{SYSTEM} = -20 \times \log \left(\sqrt{10^{\frac{-SNR_{AMP+FILTER}}{10}} + 10^{\frac{-SNR_{ADC}}{10}}} \right) \quad (12)$$

This formula shows that if the SNR of the amplifier and filter equals the SNR of the ADC, the combined SNR is 3 dB lower (worse). Thus, for minimal degradation (< 1 dB) on the ADC SNR, the SNR of the amplifier and filter must be at least 10 dB greater than the ADC SNR. The combined SNR calculated in this manner is usually accurate to within ±1 dB of the actual implementation.

10.1.7 SFDR Considerations

The SFDR of the amplifier is usually set by the second-order or third-order harmonic distortion for single-tone inputs, and by the second-order or third-order intermodulation distortion for two-tone inputs. Harmonics and second-order intermodulation distortion can be filtered to some degree, but third-order intermodulation spurs cannot be filtered. The ADC generates the same distortion products as the amplifier, but as a result of the sampling and clock feedthrough, additional spurs (not linearly related to the input signal) are included.

When the spurs from the amplifier and filter are known, each individual spur can be directly added to the same spur from the ADC, as shown in Equation 13, to estimate the combined spur (spur amplitudes in dBc):

$$HDx_{SYSTEM} = -20 \times \log\left(10^{\frac{-HDx_{AMP+FILTER}}{20}} + 10^{\frac{-HDx_{ADC}}{20}}\right) \quad (13)$$

This calculation assumes the spurs are in phase, but usually provides a good estimate of the final combined distortion.

For example, if the spur of the amplifier and filter equals the spur of the ADC, then the combined spur is 6 dB higher. To minimize the amplifier contribution (< 1 dB) to the overall system distortion, the spur from the amplifier and filter must be approximately 19 dB lower in amplitude than that of the converter. The combined spur calculated in this manner is usually accurate to within ±6 dB of the actual implementation; however, higher variations can be detected as a result of phase shift in the filter, especially in second-order harmonic performance.

This worst-case spur calculation assumes that the amplifier and filter spur of interest is in phase with the corresponding spur in the ADC, such that the two spur amplitudes can be added linearly. There are two phase-shift mechanisms that cause the measured distortion performance of the amplifier-ADC chain to deviate from the expected performance calculated using Equation 13: common-mode phase shift and differential phase shift.

Common-mode phase shift is the phase shift detected equally in both branches of the differential signal path including the filter. Common-mode phase shift nullifies the basic assumption that the amplifier, filter, and ADC spur sources are in phase. This phase shift can lead to better performance than predicted when the spurs become phase shifted, and there is the potential for cancellation when the phase shift reaches 180°. However, a significant challenge exists in designing an amplifier-ADC interface circuit to take advantage of a common-mode phase shift for cancellation: the phase characteristic of the ADC spur sources are unknown. Thus, the necessary phase shift in the filter and signal path for cancellation is also unknown.

Differential phase shift is the difference in the phase response between the two branches of the differential filter signal path. Differential phase shift in the filter as a result of mismatched components caused by nominal tolerance can severely degrade the even-order distortion of the amplifier-ADC chain. This effect has the same result as mismatched path lengths for the two differential traces, and causes more phase shift in one path than the other. Ideally, the phase response over frequency through the two sides of a differential signal path are identical, such that even-order harmonics remain optimally out of phase and cancel when the signal is taken differentially. However, if one side has more phase shift than the other, then the even-order harmonic cancellation is not as effective.

Single-order RC filters cause very little differential phase shift with nominal tolerances of 5% or less, but higher-order LC filters are very sensitive to component mismatch. For instance, a third-order Butterworth band-pass filter with a 100-MHz center frequency and a 20-MHz bandwidth creates as much as 20° of differential phase imbalance in a SPICE Monte Carlo analysis with 2% component tolerances. Therefore, although a prototype may work, production variance is unacceptable. In ac-coupled applications that require second- and higher-order filters between the LMH3404 and the ADC, use a transformer or balun at the ADC input to restore the phase balance. For dc-coupled applications where a transformer or balun at the ADC input cannot be used, use first- or second-order filters to minimize the effect of differential phase shift because of the component tolerance.

10.1.8 Driving Capacitive Loads

With high-speed signal paths, capacitive loading is highly detrimental to the signal path. Designers must make every effort to reduce parasitic loading on the amplifier output pins. The device on-chip resistors are included in order to isolate the parasitic capacitance associated with the package and the PCB pads that the device is soldered to. The LMH3404 is stable with most capacitive loads; however, bandwidth suffers with capacitive loading on the output.

10.1.9 Driving Matched Loads

The LMH3404 has on-chip output resistors; however, for most load conditions, additional resistance must be added to the output to match a desired load. Table 2 lists the matching resistors for some common load conditions. To drive unmatched loads, see the *Driving Low Insertion-Loss Filters* section.

Table 2. Load Component Values

LOAD (R_L)	R_{O+} AND R_{O-} FOR MATCHED TERMINATION	TOTAL LOAD RESISTANCE AT AMPLIFIER OUTPUT(1)	TERMINATION LOSS
50 Ω	15 Ω	100 Ω	6 dB
100 Ω	40 Ω	200 Ω	6 dB
200 Ω	90 Ω	400 Ω	6 dB
400 Ω	190 Ω	800 Ω	6 dB
1 kΩ	490 Ω	2000 Ω	6 dB

(1) The total load includes termination resistors.

10.1.10 Driving Low Insertion-Loss Filters

When driving high-speed ADCs, it is often common to drive a filter that with a matched impedance to the ADC. This impedance is matched by the amplifier by setting the combination of the output resistors to the same impedance as the ADC inputs. Impedance matching is often done to minimize any transmission reflections caused by the physical signal path. The drawback to using a matched impedance is that it demands a voltage swing from the amplifier outputs that is twice the desired ADC input voltage swing, which can cause output voltage limitation issues.

To avoid using a matched impedance, it is possible to drive a low insertion loss filter where there is little to no resistance added at the amplifier outputs. The amplifier outputs then only have to swing to the value of the ADC full scale input voltage, thus eliminating most of the potential amplifier output headroom issues. The requirements to use this technique are that the amplifier must be able to provide enough current to the load of the ADC, and that the path between the amplifier outputs and ADC inputs must be minimized to prevent any reflections.

10.1.11 Driving ADCs

The LMH3404 is designed, and optimized for the highest performance, to drive differential input ADCs.Figure 69 shows a generic block diagram of the LMH3404 driving an ADC. The primary interface circuit between the amplifier and the ADC is usually a filter for antialiasing purposes, which also provides a means to bias the signal to the input common-mode voltage required by the ADC. Filters range from single-order real RC poles to higher-order LC filters, depending on the requirements of the application. Output resistors (R_O) are shown on the amplifier outputs to isolate the amplifier from any capacitive loading presented by the filter.

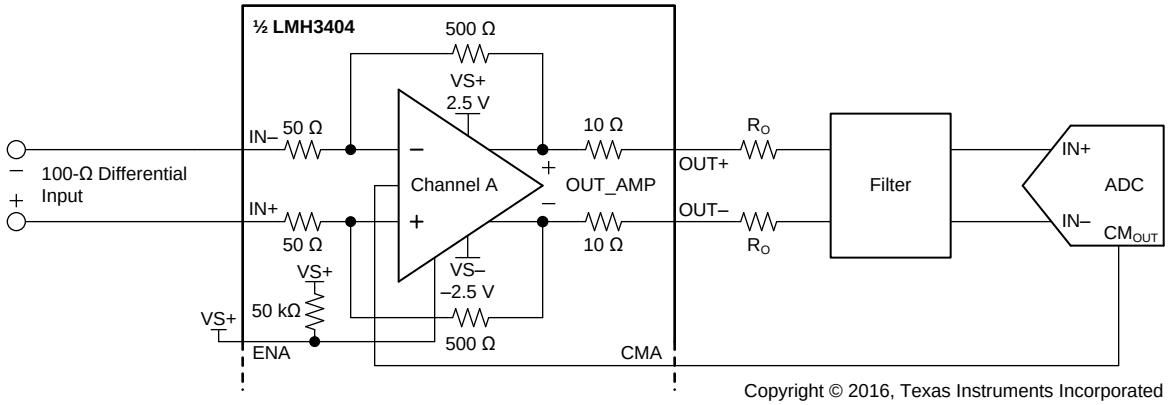


Figure 69. Differential ADC Driver Block Diagram

The key points to consider for implementation are the SNR, SFDR, and ADC input considerations, as described in this section.

10.1.11.1 ADC Input Common-Mode Voltage Considerations: AC-Coupled Input

The input common-mode voltage range of the ADC must be respected for proper operation. In an ac-coupled application between the amplifier and the ADC, the input common-mode voltage bias of the ADC is accomplished in different ways depending on the ADC. Some ADCs use internal bias networks such that the analog inputs are automatically biased to the required input common-mode voltage if the inputs are ac-coupled with capacitors (or if the filter between the amplifier and ADC is a band-pass filter). Other ADCs supply the required input common-mode voltage from a reference voltage output pin (often called CM or V_{CM}). With these ADCs, the ac-coupled input signal can be rebiased to the input common-mode voltage by connecting resistors from each input to the CM output of the ADC, as Figure 70 shows. However, the signal is attenuated because of the voltage divider created by R_{CM} and R_O.

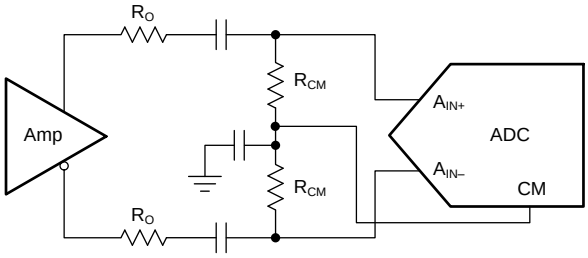


Figure 70. Biasing AC-Coupled ADC Inputs Using the ADC CM Output

The signal can be rebiased when ac coupled; thus, the output common-mode voltage of the amplifier is a *don't care* for the ADC.

10.1.11.2 ADC Input Common-Mode Voltage Considerations: DC-Coupled Input

DC-coupled applications vary in complexity and requirements, depending on the ADC. One typical requirement is resolving the mismatch between the common-mode voltage of the driving amplifier and the ADC. Devices such as the ADS5424 require a nominal 2.4-V input common-mode; whereas, other devices such as the ADS5485 require a nominal 3.1-V input common-mode; and still others, such as the ADS6149 and the ADS4149, require 1.5 V and 0.95 V, respectively. As shown in Figure 71, a resistor network can be used to perform a common-mode level shift. This resistor network consists of the amplifier series output resistors and pullup or pulldown resistors to a reference voltage. This resistor network introduces signal attenuation that may prevent the use of the full-scale input range of the ADC. ADCs with an input common-mode closer to the typical 2.5-V LMH3404 output common-mode are easier to dc-couple, and require little or no level shifting.

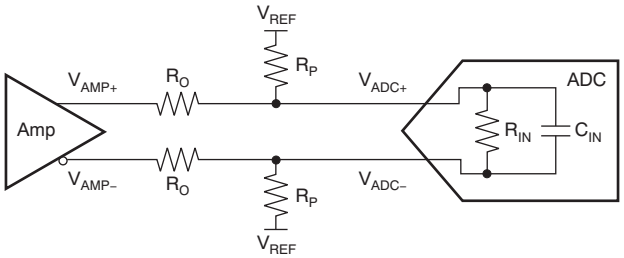


Figure 71. Resistor Network to DC Level-Shift Common-Mode Voltage

For common-mode analysis of the circuit in Figure 71, assume that $V_{AMP\pm} = V_{CM}$ and $V_{ADC\pm} = V_{CM}$ (the specification for the ADC input common-mode voltage). V_{REF} is chosen to be a voltage within the system higher than V_{CM} (such as the ADC or amplifier analog supply) or ground, depending on whether the voltage must be pulled up or down, respectively; R_O is chosen to be a reasonable value, such as 24.9 Ω. With these known values, R_P is found by using Equation 14:

$$R_P = R_O \left(\frac{V_{ADC} - V_{REF}}{V_{AMP} - V_{ADC}} \right) \tag{14}$$

Shifting the common-mode voltage with the resistor network comes at the expense of signal attenuation. Modeling the ADC input as the parallel combination of a resistance (R_{IN}) and capacitance (C_{IN}) using values taken from the ADC data sheet, the approximate differential input impedance (Z_{IN}) for the ADC is calculated at the signal frequency. The effect of C_{IN} on the overall calculation of gain is typically minimal, and can be ignored for simplicity (that is, $Z_{IN} = R_{IN}$). The ADC input impedance creates a divider with the resistor network; the gain (attenuation) for this divider can be calculated by Equation 15:

$$GAIN = \left(\frac{2R_P \parallel Z_{IN}}{2R_O + 2R_P \parallel Z_{IN}} \right) \tag{15}$$

With ADCs that have internal resistors that bias the ADC input to the ADC input common-mode voltage, the effective R_{IN} is equal to twice the value of the bias resistor. For example, the ADS5485 has a 1-kΩ resistor tying each input to the ADC V_{CM}; therefore, the effective differential R_{IN} is 2 kΩ.

The introduction of the R_P resistors also modifies the effective load that must be driven by the amplifier. Equation 16 shows the effective load created when using the R_P resistors.

$$R_L = 2R_O + 2R_P \parallel Z_{IN} \tag{16}$$

The R_P resistors function in parallel to the ADC input such that the effective load (output current) at the amplifier output is increased. Higher current loads limit the LMH3404 differential output swing.

By using the gain and knowing the full-scale input of the ADC ($V_{ADC\ FS}$), the required amplitude to drive the ADC with the network is calculated using Equation 17:

$$V_{AMP\ PP} = \frac{V_{ADC\ FS}}{GAIN} \tag{17}$$

As with any design, testing is recommended to validate whether the specific design goals are met.

10.1.11.3 Common-Mode Voltage Correction

The LMH3404 can set the output common-mode voltage to within a typical value of ±30 mV. If greater accuracy is desired, a simple circuit can improve this accuracy by an order of magnitude. A precision, low-power operational amplifier is used to sense the error in the output common-mode voltage of the LMH3404, and corrects the error by adjusting the voltage at the CMA or CMB pin. In Figure 72, the precision of the op amp replaces the less accurate precision of the LMH3404 common-mode control circuit, while still using the LMH3404 common-mode control circuit speed. The op amp in this circuit must have better than a 1-mV input-referred offset voltage and low noise. Otherwise, the specifications are not very critical because the LMH3404 is responsible for the entire differential signal path.

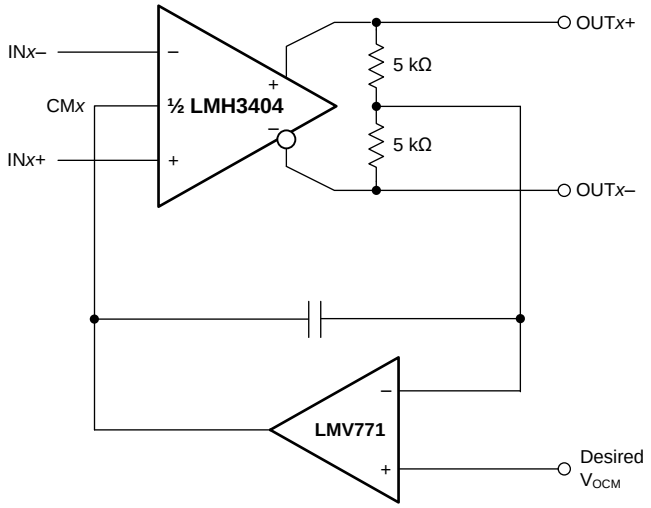


Figure 72. Common-Mode Correction Circuit

10.2 Typical Applications

10.2.1 Active Balun

The LMH3404 converts single-ended signals to a differential output with very high bandwidth and linearity, as shown in Figure 73. The LMH3404 can support dc coupling, as well as ac coupling. The LMH3404 is smaller than any balun with low-frequency response, and has balance errors that are excellent over a wide frequency range. As shown in Figure 74, the LMH3404 balance error is better than –35 dBc up to 1 GHz when used with a 5-V supply. Figure 75 plots the input return loss. The S-parameters demonstrate the performance of the configuration, which is comparable to (or even better than) a balun.

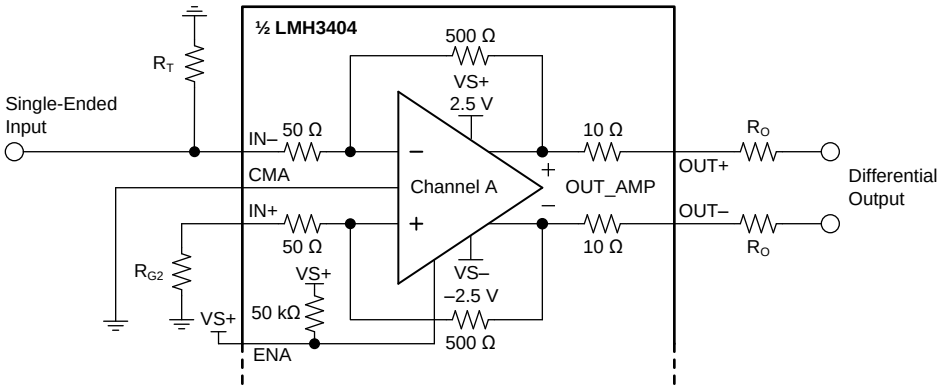


Figure 73. Active Balun

10.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Supply voltage	±2.5 V
Common-Mode voltage	0 V
Voltage gain	7.9 V/V
Source resistance	50 Ω
Input termination resistor (R_T)	90.9 Ω
Input balancing resistor (R_{G2})	31.6 Ω
Operating frequency	DC up to 1 GHz

10.2.1.2 Detailed Design Procedure

To begin the design process, make sure that none of the following design parameters exceed the limits listed in the *Electrical Characteristics* table.

- Output voltage range
- Output current rating
- Maximum operating frequency
- Output common-mode voltage (as set by the CMA or CMB pin)
- Supply voltage

10.2.1.2.1 Source Resistance Matching

For the active balun configuration, make sure to choose the correct R_T and R_{G2} resistors in order to match the impedance of the connected single-ended source. Table 3 shows example values to match a single-ended, 50-Ω source impedance. If the design uses a source with a different impedance, recalculate the R_T and R_{G2} values by following the steps outlined in the *Resistor Design Equations for Single-to-Differential Applications* section.

10.2.1.2.2 Output Common-Mode Control

For the best performance and highest output voltage range, tie the output common-mode control pin (CMA or CMB) to midsupply. If a different output common-mode voltage is required, change the voltage on the common-mode control pin to the desired value.

10.2.1.2.3 Input Common-Mode Voltage

For a dc-coupled application, the input common-mode voltage is set by the combination of the output-common mode voltage and any dc common-mode voltage present on the input signal. If these voltages are not equal, the signal source must be able to source or sink the resulting dc common-mode current that flows through the feedback network. Also, the RT and RG2 resistors need to be terminated to the input-common mode level of the DC source.

For ac-coupled applications, the input common-mode voltage is set by the output common-mode voltage. In this case, the input common-mode voltage is determined only by the value of the output-common mode. Input resistors R_T and R_{G2} must be terminated to the same voltage as the output common-mode voltage. Otherwise, the voltage mismatch causes a dc offset voltage between the two differential outputs.

10.2.1.2.4 Choosing Series Output Resistors (R_O)

The LMH3404 exhibits the best performance when driving a total load resistance of 200 Ω. If possible, choose series output resistors that create a total load equal to 200 Ω, including the internal 10-Ω resistors on each output. If the load is already greater than 200 Ω, then the series output resistors can be omitted if the device is not required to drive a matched-impedance transmission line. If the device is driving a matched-impedance transmission line, make sure to match the characteristic impedance of the line using the series output resistors (include the internal 10-Ω resistors) to minimize reflection losses. If the total load resistance presented to the device is too high, the outputs start to clip. In this case, either add a resistor in parallel with the load resistance to reduce the total effective load, or reduce the output signal swing voltage.

10.2.1.3 Application Curves

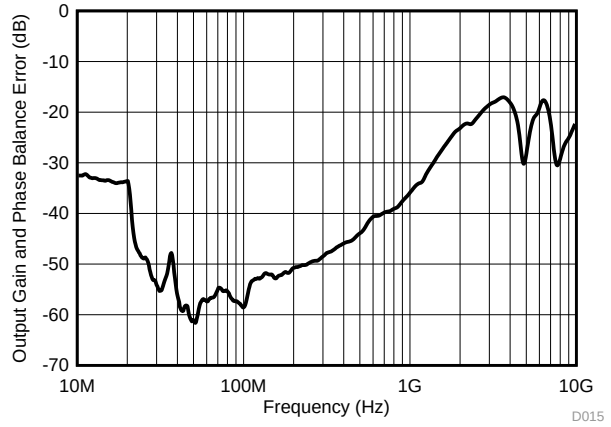


Figure 74. SE-Diff Balance Error

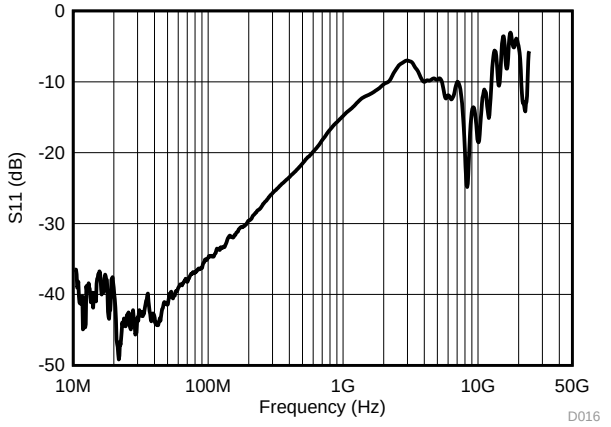


Figure 75. SE-Diff Input Return Loss

10.2.2 Single-Ended Input ADC Driver

A typical application driving an ADC is shown in Figure 76.

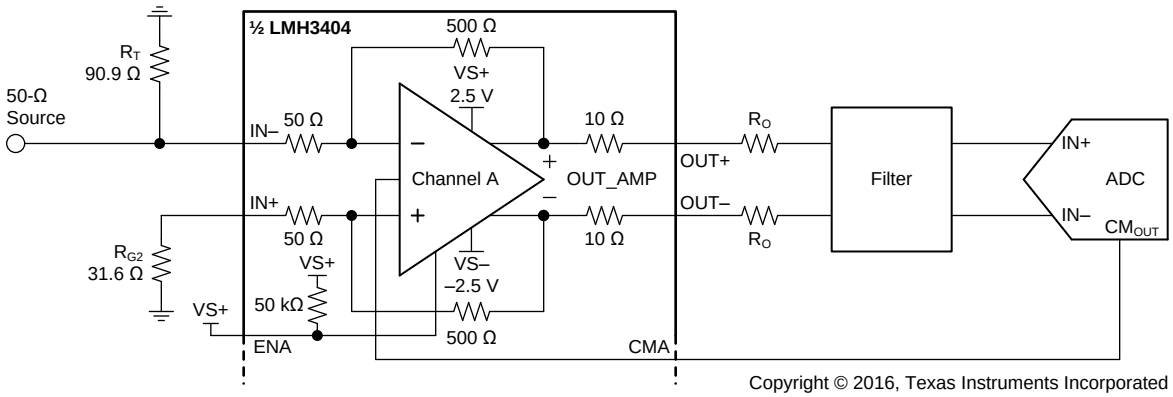


Figure 76. Single-Ended Input ADC Driver

The LMH3404 is designed as a single-ended-to-differential (SE-Diff) and differential-to-differential (Diff-Diff) gain block configured with internally set resistors. The LMH3404 has no low-end frequency cutoff, and has 7-GHz small-signal bandwidth (SSBW). The LMH3404 is a very attractive substitute for a balun transformer in many applications.

The resistors labeled R_O serve to match the filter impedance to the 20-Ω amplifier differential output impedance. If no filter is used, these resistors may not be required if the ADC is located very close to the LMH3404. If there is a transmission line between the LMH3404 and the ADC, then the R_O resistors must be sized to match the transmission-line impedance.

10.2.2.1 Design Requirements

The main design requirements are to keep the amplifier input and output common-mode voltages compatible with the ADC requirements and the amplifier requirements. Split power supplies are used for this application example.

10.2.3 GSPS ADC Driver

The LMH3404 can drive the full Nyquist bandwidth of ADCs with sampling rates up to 4 GSPS, as shown in Figure 77. If the front-end bandwidth of the ADC is more than 2 GHz, use a simple noise filter to improve SNR. Otherwise, the ADC can be connected directly to the amplifier output pins. Matching resistors may not be required; however, allow space for matching resistors on the preliminary design.

Some high-speed ADCs have low input impedance (< 100 Ω) in order to achieve high bandwidths. To drive a low-impedance ADC, it is best to add series resistors to increase the effective load of the amplifier as close as possible to a value of 200 Ω. However, be aware that adding series resistance increases the voltage swing from the amplifier outputs to drive an equivalent ADC full-scale input voltage. Too much series resistance also causes the outputs to clip.

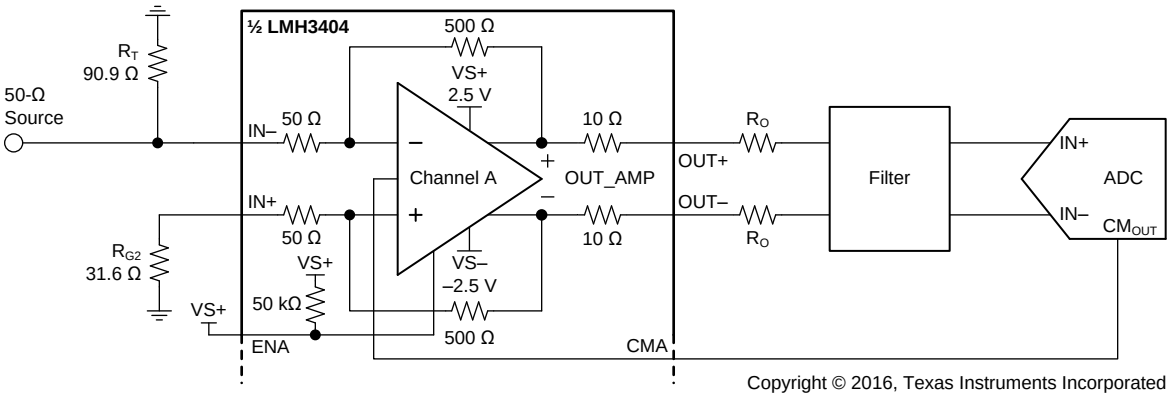


Figure 77. GSPS ADC Driver

10.2.4 IQ Receiver ADC Driver

The LMH3404 is a dual channel device; therefore this device has excellent gain and phase matching between channels A and B. This matching makes the LMH3404 an excellent choice for systems that require two matched channels, such as an IQ demodulation receiver, as shown in figure Figure 78 using the LMH3404 and ADC32RF45 dual channel, 14-bit, 3.0 GSPS ADC. For an IQ system, it is important that both the gain and phase match for the real and imaginary channel. When using two single-channel amplifiers, the matching characteristics are subject to process lot and packaging variations for two individual chips, and there is often no way to make sure the amplifiers will match without testing each amplifier. However, the dual-channel architecture of the LMH3404 allows for much tighter gain and phase matching of 0.04 dB and 0.7°, respectively. For more matching information, see the *Electrical Characteristics: V_S = 5 V* and *Electrical Characteristics: V_S = 3.3 V* tables. For a reference design example of the LMH3404 used with the ADC32RF45 in a complex digitizer application, go to http://www.ti.com/tool/TIDA-00813.

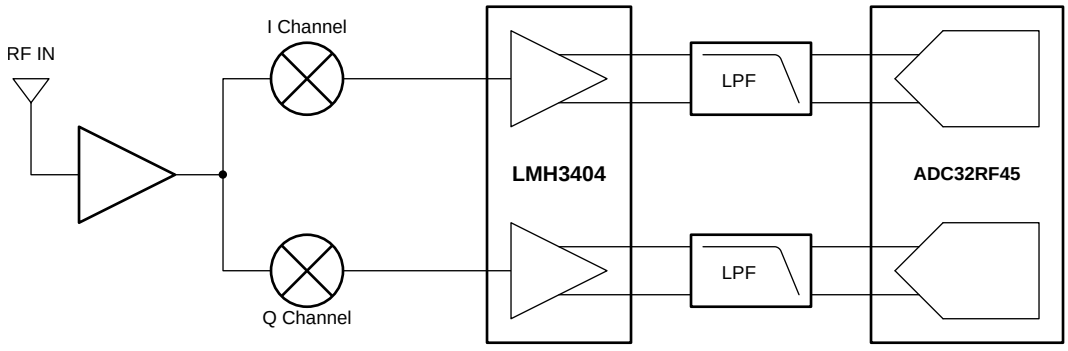


Figure 78. IQ Receiver Block Diagram

10.3 Do's and Don'ts

10.3.1 Do's

- Do include a thermal design at the beginning of the project.
- Do use well-terminated transmission lines for all signals.
- Do use solid metal layers for the power supplies.
- Do keep signal lines as straight as possible.
- Do use split supplies where required.

10.3.2 Don'ts

- Don't use a lower supply voltage than necessary.
- Don't use thin metal traces to supply power.
- Don't forget about the common-mode response of filters and transmission lines.

11 Power-Supply Recommendations

The LMH3404 can be used with either split or single-ended power supplies. The ideal supply voltage is a 5.0-V total supply, split around the desired common-mode of the output signal swing. For example, if the LMH3404 is used to drive an ADC with a 1.0-V input common mode, then the ideal supply voltages are 3.5 V and –1.5 V. The GND pin can then be connected to the system ground, and the enable pin is ground referenced.

11.1 Supply Voltage

Use a 5-V power supply to give the best balance of performance and power dissipation. If power dissipation is a critical design criteria, a power supply as low as 3.3 V (±1.65) can be used. When using a lower power supply, the input common-mode and output swing capabilities are drastically reduced. Make sure to study the common-mode voltages required before deciding on a lower-voltage power supply. In most cases, the extra performance achieved with 5-V supplies is worth the power.

11.2 Single Supply

Single-supply voltages from 3.3 V to 5 V are supported. When using a single supply, check both the input and output common-mode voltages that are required by the system.

11.3 Split Supply

In general, split supplies allow the most flexibility in system design. To operate as split supply, apply the positive supply voltage to VS+, the negative supply voltage to VS–, and the ground reference to the thermal pad voltage (ground). Supply voltages do not need to be symmetrical. Provided the total supply voltage is between 3.3 V and 5.25 V, any combination of positive and negative supply voltages is acceptable. This feature is often used when the output common-mode voltage must be set to a particular value. For best performance, make sure the power-supply voltages are symmetrical around the desired output common-mode voltage. The input common-mode voltage range is much more flexible than the output common-mode voltage range.

11.4 Supply Decoupling

Power-supply decoupling is critical to high-frequency performance. Onboard bypass capacitors are used on the LMH3404EVM; however, the most important component of the supply bypassing is provided by the PCB. As illustrated in Figure 79, there are multiple vias connecting the LMH3404 power planes to the power-supply traces. These vias connect the internal power planes to the LMH3404. Both VS+ and VS– must be connected to the internal power planes with several square centimeters of continuous plane in the immediate vicinity of the amplifier. The capacitance between these power planes provides the bulk of the high-frequency bypassing for the LMH3404.

The EVM also includes a 5.1-nH inductor in series with the positive power supply. This inductor serves to filter out second-order distortion components that are present on the positive power supply. For narrow-band applications, it is possible to tune this inductor to maximize second-order performance at a specific frequency. However, the inductor will potentially degrade performance at other frequencies, and therefore should not be altered for wide-band applications. The part also functions with no inductor at the cost of some second-order harmonic performance.

12 Layout

12.1 Layout Guidelines

With a small signal bandwidth of 7 GHz, layout for the LMH3404 is critical, and nothing can be neglected. In order to simplify board design, the LMH3404 has on-chip resistors that reduce the affect of off-chip capacitance. For this reason, make sure that the ground layer below the LMH3404 is not cut. The recommendation to not cut the ground plane under the amplifier input and output pins is different than many other high-speed amplifiers, but the reason is that parasitic inductance is more harmful to the LMH3404 performance than parasitic capacitance. By leaving the ground layer under the device intact, parasitic inductance of the output and power traces is minimized. The DUT portion of the evaluation board layout is illustrated in Figure 79.

The EVM uses long-edge capacitors for the decoupling capacitors, which reduces series resistance and increases the resonant frequency. Vias are also placed to the power planes before the bypass capacitors. Although not evident in the top layer, two vias are used at the capacitor in addition to the two vias underneath the device.

The output matching resistors are 0402 size and are placed very close to the amplifier output pins, which reduces both parasitic inductance and capacitance. The use of 0603 output matching resistors produces a measurable decrease in bandwidth.

When the signal is on a 50-Ω controlled impedance transmission line, the layout then becomes much less critical. The transition from the 50-Ω transmission line to the amplifier pins is the most critical area.

The CMA or CMB pin also requires a bypass capacitor. Place this capacitor near the device. Refer to the *LMH3404EVM Evaluation Module User's Guide* (SBOU124) for more details on board layout and design.

12.2 Layout Example

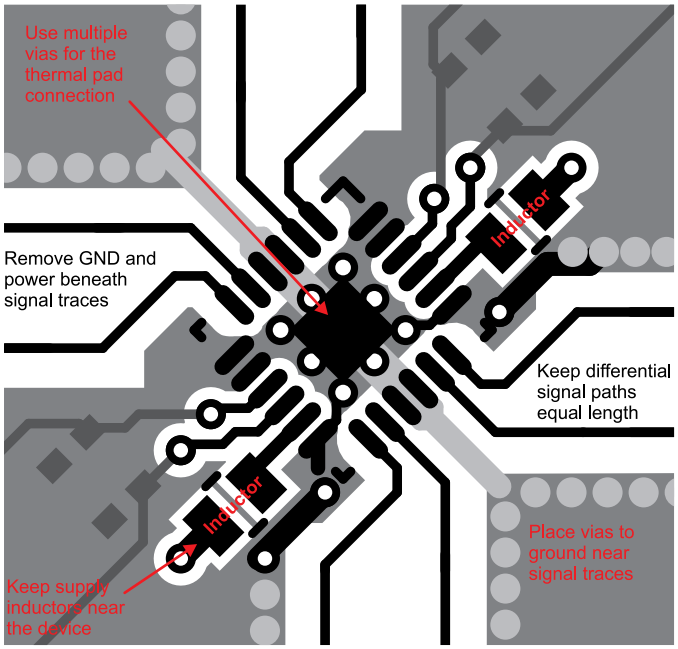


Figure 79. Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 Device Nomenclature

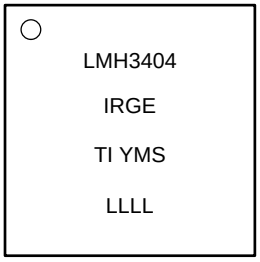


Figure 80. Device Marking Information

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- *LMH3401 7-GHz, Ultra-Wideband, Fixed-Gain, Fully-Differential Amplifier Data Sheet* (SBOS695)
- *LMH5401 8-GHz, Low-Noise, Low-Power, Fully-Differential Amplifier Data Sheet* (SBOS710)
- *LMH6552 1.5-GHz Fully Differential Amplifier Data Sheet* (SNOSAX9)
- *LMH6554 2.8-GHz Ultra Linear Fully Differential Amplifier Data Sheet* (SNOSB30)
- *ADC12D1800RF 12 Bit, Single 3.6 GSPS RF Sampling ADC Data Sheet* (SNAS518)
- *ADS5424 14-Bit, 105-MSPS Analog-to-Digital Converter Data Sheet* (SLWS157)
- *ADS5485 16-Bit, 170-MSPS and 200-MSPS Analog-to-Digital Converters Data Sheet* (SLAS610)
- *ADS6149 14/12-Bit, 250/210MSPS ADCs With DDR LVDS and Parallel CMOS Outputs Data Sheet* (SLWS211)
- *ADS4149 12-Bit and 14-Bit, 160-MSPS and 250-MSPS, Ultralow-Power ADC Data Sheet* (SBAS483)
- *LMH3404EVM Evaluation Module User's Guide* (SBOU124)
- *AN-2188 Between the Amplifier and the ADC: Managing Filter Loss in Communications Systems Application Report* (SNOA567)
- *AN-2235 Circuit Board Design for LMH6517/21/22 and Other High-Speed IF/RF Feedback Amplifiers Application Report* (SNOA869)
- *LMH3404 TINA Model* (SBOM920)

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH3404IRGER	PREVIEW	VQFN	RGE	24	3000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LMH3404 IRGE	
LMH3404IRGET	PREVIEW	VQFN	RGE	24	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LMH3404 IRGE	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

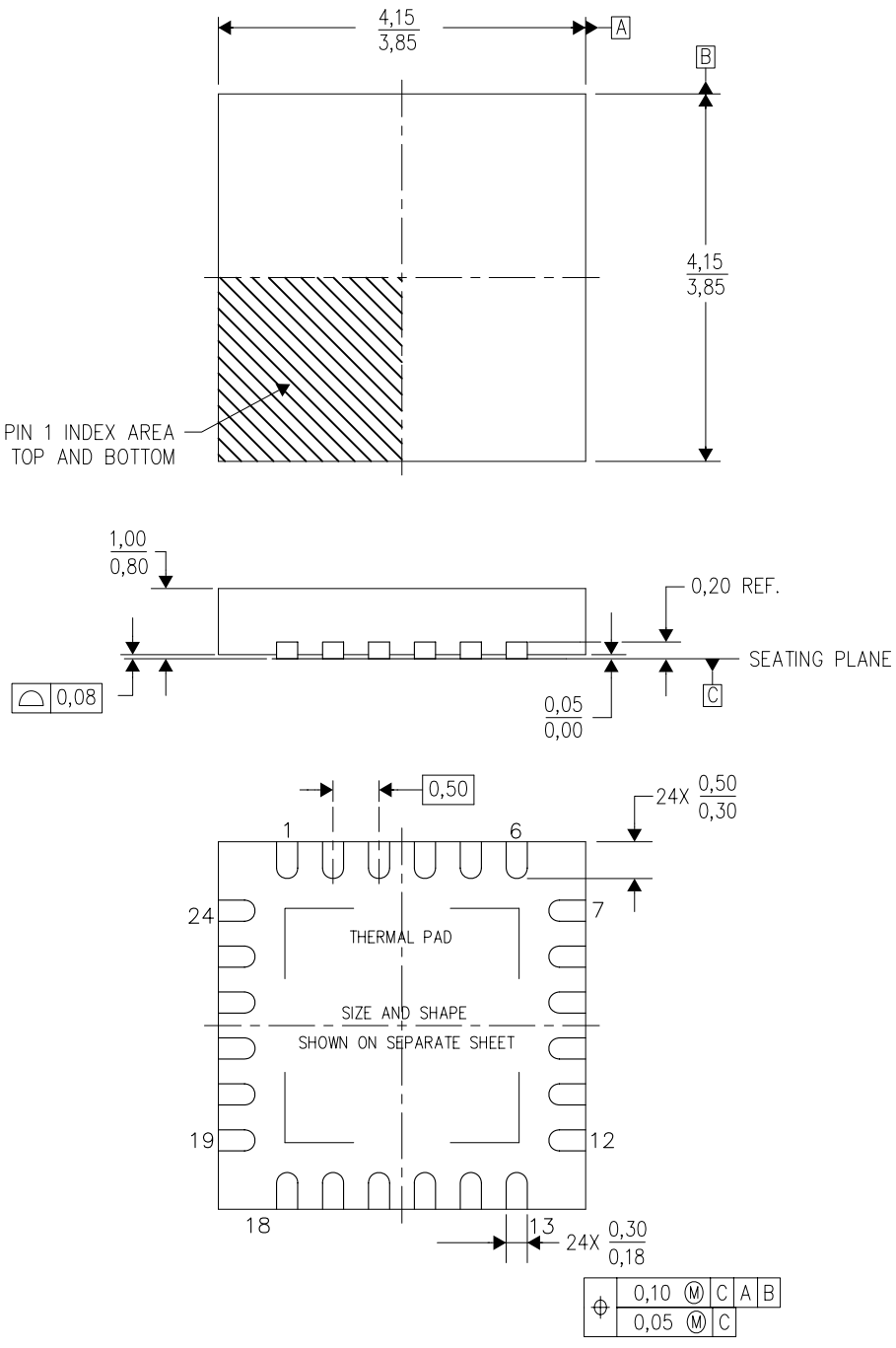
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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